

# **Past and Future of Silicon Electronic Devices**

**@Xian Jiaotong University**

**December 24, 2009**

**東京工業大学**

**Tokyo Institute of Technology**

**先端研究中心**

**Frontier Research Center**

**岩井 洋 Hiroshi Iwai,**



**Tokyo Institute of Technology**  
**Founded in 1881, Promoted to Univ. 1929**

# Institute Overview



**Established in 1881** → 130th anniversary in 2011

**3 undergraduate schools**

School of Science, School of Engineering, School of Bioscience and Biotechnology

Einstein Visit

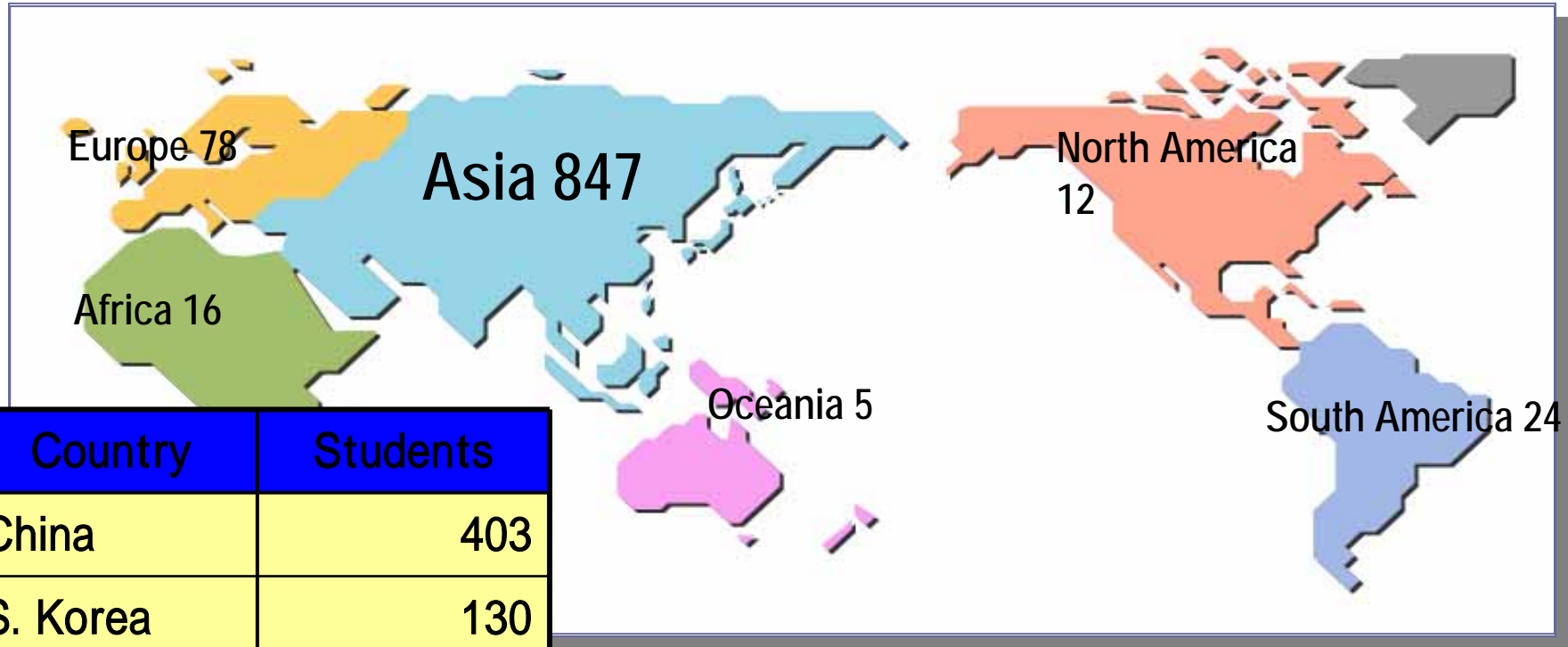
**7 graduate schools**

Science and Engineering Science, Science and Engineering Technology,  
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,  
Information Science and Engineering, Decision Science and Technology, Innovation Management

**Total Number of Students**

	Undergraduate	Graduate	Master's	Doctoral	Teaching Staff	Student/Instructor	Staff
<b>Tokyo Inst.</b>	<b>5,000</b>	<b>5,000</b>	<b>3,500</b>	<b>1,500</b>	<b>1,200</b>	<b>8.3</b>	<b>550</b>
<b>Per Year</b>	<b>1,200</b>		<b>1,800</b>	<b>500</b>			

# International Students



Country	Students
China	403
S. Korea	130
Indonesia	64
Thailand	55
Vietnam	60
Malaysia	28

**Total 982**  
(As of May. 1, 2005)

**Tokyo Institute of Technology**  
東京工業大学

2 major campuses      5000 Under graduate students  
Ookayama, Tokyo      5000 Graduate Students  
Suzukakedai, Yokohama

**Interdisciplinary Graduate School  
of  
Science and Engineering**

大学院総合理工学研究科

5 other schools

4 Laboratories

**Frontier Research Center**  
先端研究中心

Consists of about 10 professor who  
have big projects

**G CEO (Global Center of Excellence)  
for Photonics Nanodevice Integration Engineering**

Other GCEO

Consists of 5 EE  
Related departments

Innovation Research Initiatives (革新的研究集団)

**Dept. of Electronics  
and Physics**

物理電子System創造専攻

10 other dept.

# 岩井研メンバー

(2009年11月1日現在)



教授  
岩井洋



准教授(共同研究)  
筒井一生



客員教授  
Simon Min Sze



客員教授  
服部健雄



特任教授  
名取研二



連携教授  
杉井信之



連携教授  
西山彰



特任准教授  
Parhat Ahmet



助教  
角嶋邦之

## 博士 研究員



Milan Kumar Bera

## 博士 課程



D3 佐々木雄一朗



D3 下村浩



D3 宋在烈



D3 館喜一



D2 川那子高暢



D2 佐藤創志



D2 富田隆治



D2 Maimaitirexiati Maimaiti



D2 Maimaitirexiati Maimaiti



D2 Abudukeimu Abudureheman



D1 幸田みゆき



D1 李映焯



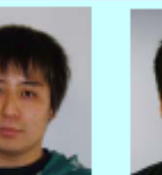
博士課程 D3 小林勇介



## 修士 課程



M2 新井英朗



M2 中山寛人



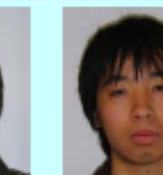
M2 船水清永



M2 細田亘



M2 又野克哉



M2 又野克哉



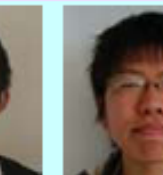
M2 タリウス・ハサンザデ



M2 Mokhammad Sholihul Hadi



M1 小柳友常



M1 小澤健児



M1 神田高志



M1 澤田剛伸



M1 茂森直登



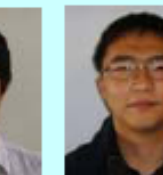
M1 向井弘樹



M1 呉研



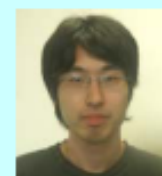
M1 Dou Chunmeng



M1 Dou Chunmeng



博士課程 M2 横田知之



博士課程 M2 星野憲文



博士課程 M1 田中正興



## 学部



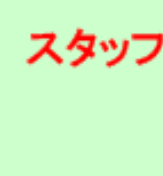
B4 来山大祐



## 研究生



Rena Salmatti



## スタッフ



松本昭子



辛川美琴



西澤 正子

Interdisciplinary Graduate School of  
Science and Engineering  
大学院総合理工学研究科

J2 Building:



Frontier Collaborative Research Center ( FCRC )  
先端創造共同研究中心





# Iwai Lab. Equipment



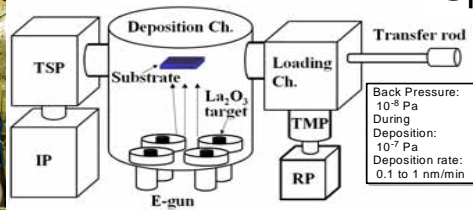
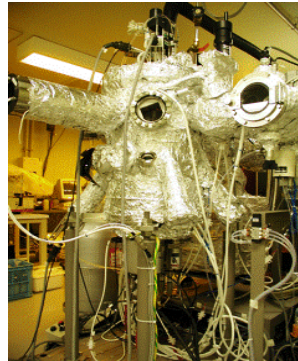
MBE and Sputter Chamber



Sputter Chamber



1/f noise measurement system; 6 inch wafer



MBE Chamber



RTA Furnace No.1



RTA Furnace No.2



RF measurement system; 8 inch wafer, 40 GHz

# 岩井研究室 ~Iwai Lab.~

## ● ご挨拶



### Welcome to Iwai Lab.

総合理工学研究所 物理電子システム創造専攻 岩井研究室

当研究室では、シリコンをベースとした集積回路のデバイス技術、特に素子超微細化や集積回路境界の探索、研究や、新材料や三次元トランジスタ構造のシリコン集積回路への導入を行っています。さらにエマージング技術としてゲルマニウムやIII-V族半導体チャネル材料の検討などを行っています。

LSI (Large scale Integrated Circuit, 大規模集積回路)の最初の製品とみなされるIntelの1k bit DRAMが製造されてから30年近くになりますが、この間にLSIは実に長足の発展を遂げ、高度な計算を行い動作や情報を制御する中核部品としてありとあらゆる機器に用いられるようになってきました。

最近のMobile Telephone, Mobile PC, ひいてはインターネットの爆発的な普及も軽量、小型、低消費電力で極めてきたことによるものです。今後更にこの文明飛躍的な発展を遂げて、近い将来人間の知性、感性の機能を代行する機器が出現することが大いに期待されます。

これはこれからの高齢化社会で予想される労働人口不足、老人介護人口不足などの状況のもとで、各人が平等にある程度以上の生活レベルを確保するためには行く行くは超えなければならないハードルであると考えますが、何れにせよこれを実現するためには現状のものから何れも性能の高い機器の実現が必要であると考えられており、まずはハードとしてのLSIの発展が今後何十年かにわたって継続していくことが必要条件のひとつと考えられています。

さて、LSIの発展はトランジスタを中心としたLSI中の素子の微細化によってなされてきましたが、トランジスタの微細化の限界がどこにあるかが重要な疑問としてクローズアップされてきます。この流れが今後も続くとする2005年頃にはゲート長が30nmとなり、更に今世紀の半ばにはゲート長はシリコン結晶中の原子の間隔である0.00035 μm(即ち3 Å)となる計算となります。この寸法切りが原子を用いてトランジスタを形成する限りにおいて究極的な限界と考えられますが、このようなゲート長のトランジスタが動作するかどうかは甚だ疑問であると思われており、経済的要因からはもう少し大きいところとも言われています。

研究テーマとしてはCMOS LSIの素子微細化の限界を見極めて、今後のLSIがハード、ソフトの両面から継続して発展していくためにはどういった技術を開発していくべきかを考えつつ、まずは微細シリコントランジスタ微細の特性研究、微細化限界とその打破(高誘電体ゲート絶縁膜などの新材料の導入、構造の改良等)の研究などから手を染めていきたいと考えています。またその後のポストスケール時代に対応した、エマージング技術として、ゲルマニウムやIII-V族半導体チャネル材料、シリコンナノワイヤートランジスタの研究を行っていると思っています。また、成果をできるだけ広く産業界に使っていただき、社会に貢献することを目指しており、産学連携と国際協力を研究の基本としています。

## 外部機関との連携研究



## ● 次世代高性能半導体デバイスに向けた研究テーマ

### Siデバイスの重要性

現代社会: 生産、金融、運輸、医療、行政などの社会機構  
インターネット、I-mode、Bluetooth、携帯電話、カーナビ、ゲーム、自動車、航空機、製造装置などの全ての機器、CD、DVDなどの娯楽

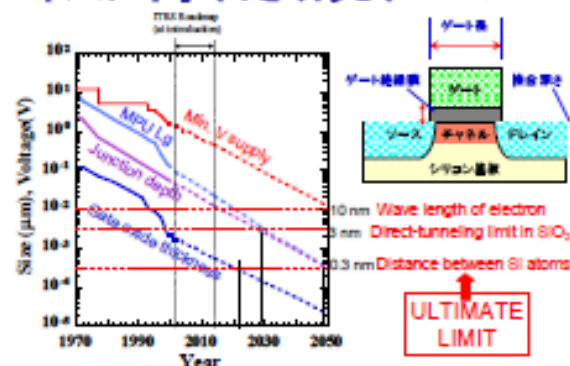
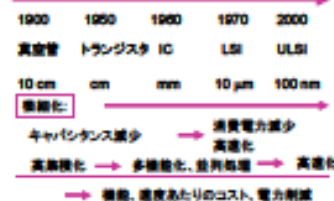
Si集積回路による管理・制御無くしてこれらは有り得ない

### 近年のSiデバイスの驚異的な発展

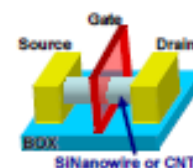
数千万個~数億個のトランジスタ集積  
MPUのクロック周波数 3GHz  
SiGeバイポーラの $f_t$  300GHz以上

### 微細化の重要性

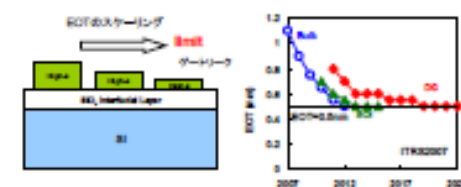
素子の微細化 (100年間で100万分の1に！)



- 低消費電力化
- 高速度
- 集積化
- パラツキ低減



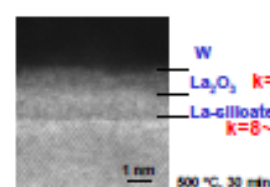
## High-k/Metalゲートスタック



高性能化・低消費電力化には EOT=0.5nmが必須

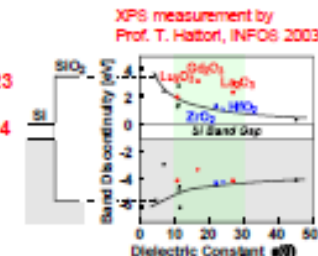
High-kとSiの直接接合が必要

## 次世代ゲート絶縁膜材料として La<sub>2</sub>O<sub>3</sub>に注目



La<sub>2</sub>O<sub>3</sub>は特性の良い直接接合が可能

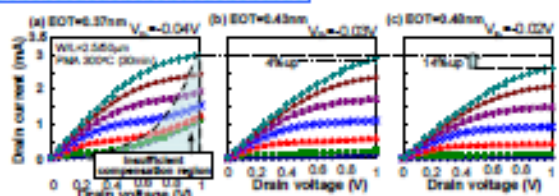
$$C_{ox} = \frac{\epsilon_d \epsilon_0}{t_{ox}} = \frac{\epsilon_{SiO_2} \epsilon_0}{EOT} \Rightarrow t_{ox} = \frac{\epsilon_d}{\epsilon_{SiO_2}} EOT$$



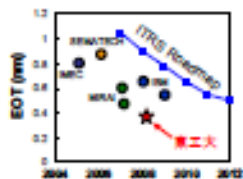
EOT: SiO<sub>2</sub>等価換算膜厚

## High-kゲート絶縁膜

EOT<0.4nmを達成

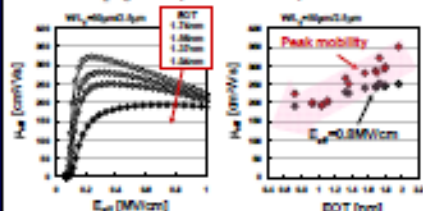


EOTの更なるスケールアップでドレイン電流増加を確認



## 低EOTにおける移動度劣化

W/La<sub>2</sub>O<sub>3</sub>/nFET, 500°C anneal, 30min in FG



直接接合で高い移動度を実現

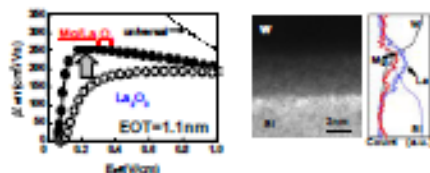
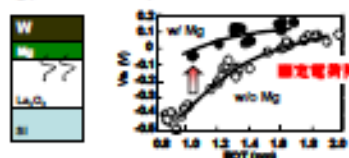


ゲート金属電極に起因する Coulomb散乱源の影響

## 低EOTの移動度向上技術

異種材料導入による低いEOTの移動度改善が可能

Mg(マグネシウム)の導入



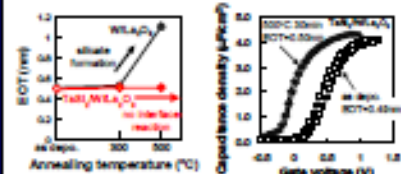
## 極限EOTに向けた材料選択

### Metal Gate

TaSi<sub>2</sub>を積層することで酸素の侵入を抑制

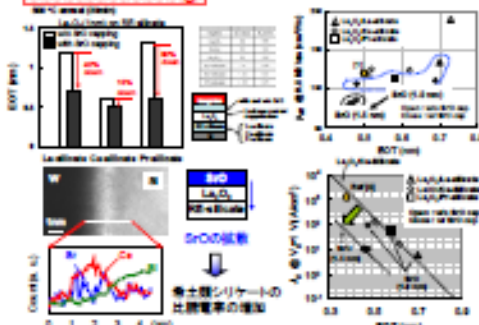
界面反応の抑制

500°CでEOT=0.5nmを達成



### k-value boosting

Ce-silicateとSrO-cappingによって0.5nm EOTを達成



## ゲルマニウムMOSFET

デバイスの更なる高速化のためにCMOSデバイスのチャンネル材料としてGeが目

ゲート長縮小の限界



ソース・ドレイン間の漏れ電流増加

	μ <sub>n</sub> [cm <sup>2</sup> /Vs]	μ <sub>p</sub> [cm <sup>2</sup> /Vs]
Si	1400	450
Ge	3900	1900
GeAs	8500	400
InP	4600	850

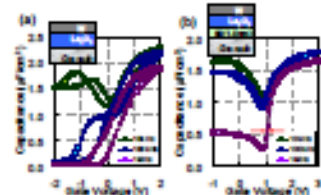
## Geトランジスタのゲート絶縁膜

GeO<sub>2</sub>は

- ①高温熱処理で分解
  - ②水溶性(ウェットプロセス不可能)
  - ③比誘電率が低い
- 良好なトランジスタ特性が得られない

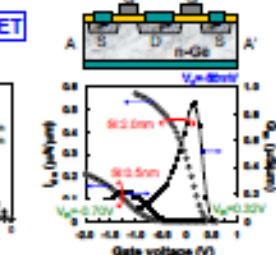
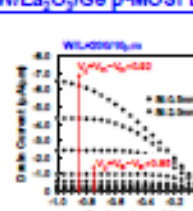
high-kをGeトランジスタのゲート絶縁膜として使おう!

High-k/Ge界面の制御が重要



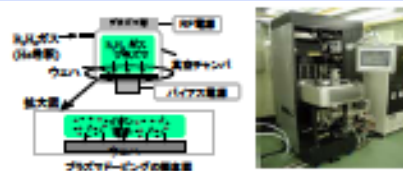
極薄Si挿入によりヒステリシスの低減が可能

## W/La<sub>2</sub>O<sub>3</sub>/Ge p-MOSFET

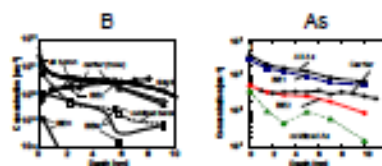


High-k/Geトランジスタの動作を確認

## 極浅接合用プラズマドーピング技術



Bの場合とAsの場合



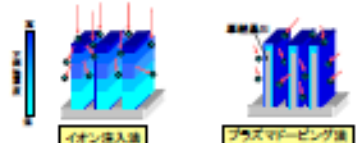
- 低エネルギー注入(~100V)
- 高いスループット(10<sup>19</sup>cm<sup>-2</sup>を30sec以内で注入可能)
- チャネリング無し→立体MOSFETに適用可能

Fin構造へのプラズマドーピング

極浅接合と高活性化の実現



4nmの接合深さを実現  
30%以上の高活性化率



Fin構造へのプラズマドーピング

- Fin構造へのプラズマドーピング
- Fin構造へのプラズマドーピング
- Fin構造へのプラズマドーピング

## SiNanowireトランジスタ

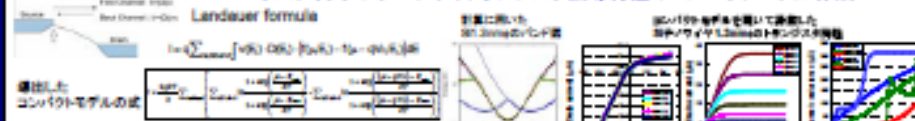
Off電流抑制の要求からナノワイヤ系FETへ

スケージングによらない低消費電力化・高性能化

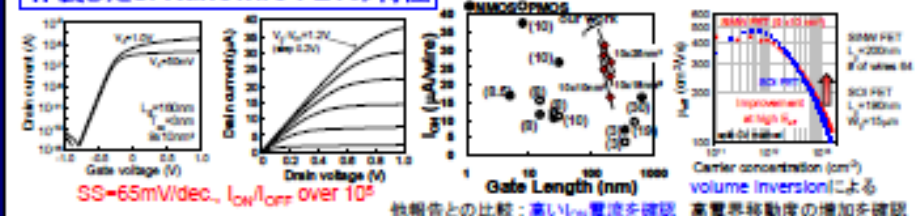


オフ電流  
・サブシュレショルドドレック電流の抑制  
オン電流  
・短チャネル速度によるドレイン電流増加  
・次元構造による量子効果

パリスティックSiナノワイヤトランジスタ伝導特性のコンパクトモデル作成

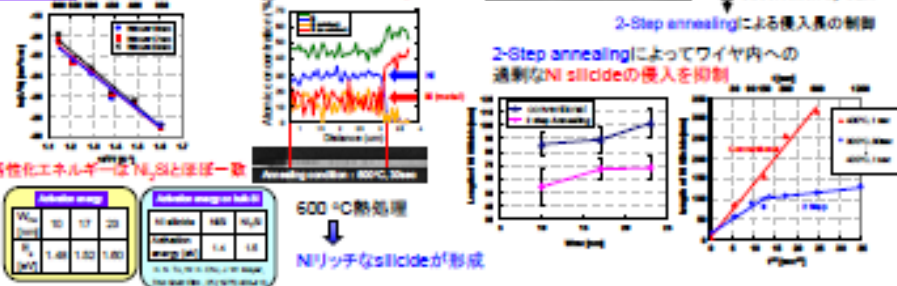


## 作製したSi Nanowire FETの特性



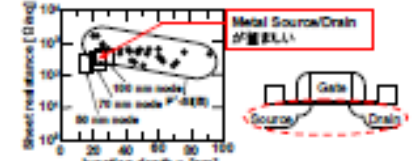
## Si NanowireのNiシリサイド化

Si Nanowire FETのSource/Drain領域の寄生抵抗  
 $I_{ON}$ 電流の減少  
Ni silicideが有効  
Si Nanowire  
Ni silicide形成機構の理解  
Ni silicideの侵入の制御



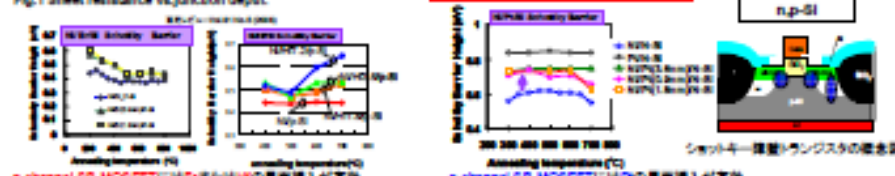
## ショットキー障壁トランジスタ

Source/Drain領域のスケージング



- 利点
- 薄い接合形成が容易
  - ソース/ドレイン低抵抗
  - 短チャネル効果耐性が高い
- 欠点
- ショットキー障壁による駆動電流の劣化

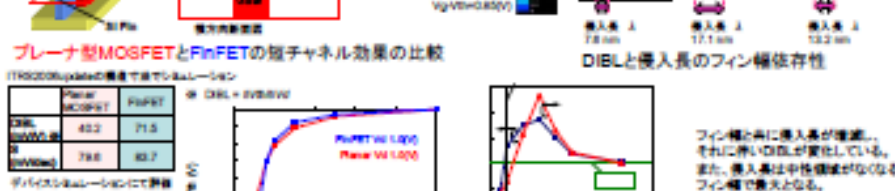
Schottky障壁の制御が必要



## ロバスト3次元トランジスタ

FinFETの微細化により生じる諸問題の明確化と改善

ドレインからの電界の侵入



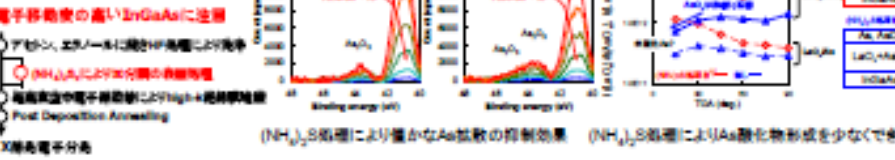
FinFETの方が短チャネル効果に強い。問題1?

フィン幅をゲート長の2/3よりも狭くしないと短チャネル効果を十分抑えられない。

## III-V族半導体

更なる高速化のためには新たなチャネル材料が必要

電子移動度の高いInGaAsに注目

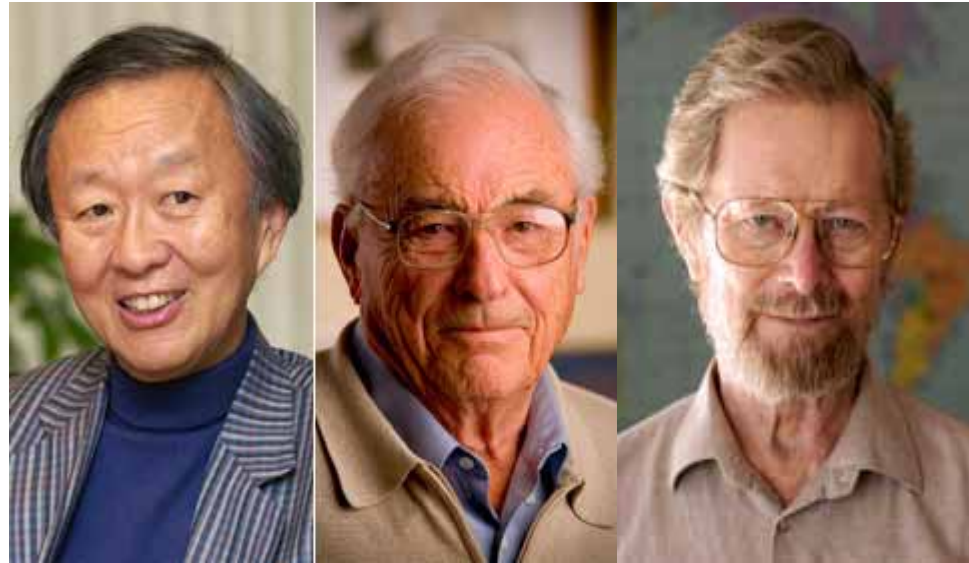




By Dr. Lu Terman, at IEDM 2009

# Three IEEE Fellows Win 2009 Nobel Prize in Physics

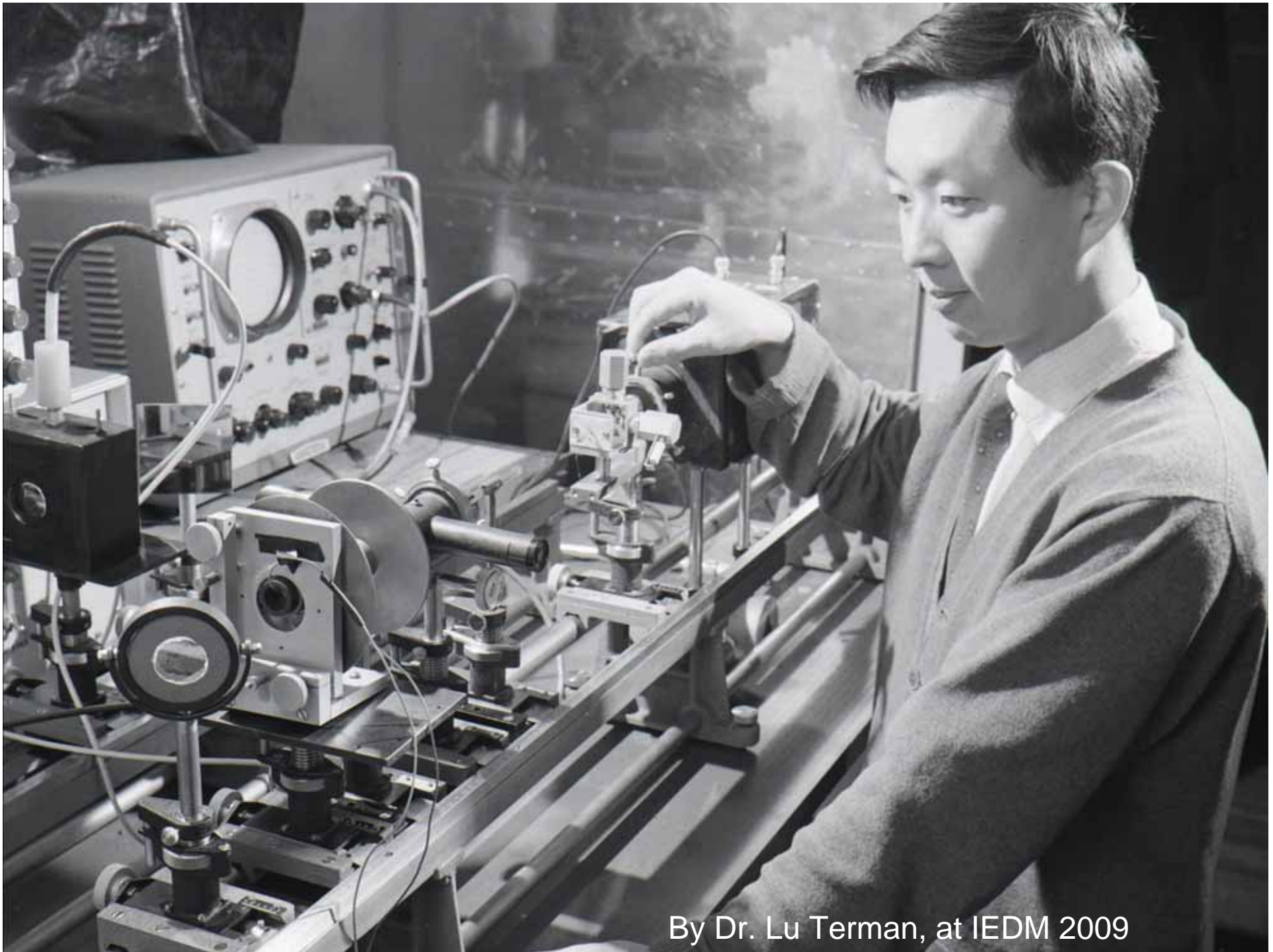
**“...for breakthroughs involving the transmission of light in fiber optics and inventing an imaging semiconductor circuit, the three scientists created the technology behind digital photography and helped link the world through fiber optic networks.”**



**(l-r)  
Dr. Charles K. Kao  
Dr. Willard S. Boyle  
Dr. George E. Smith**

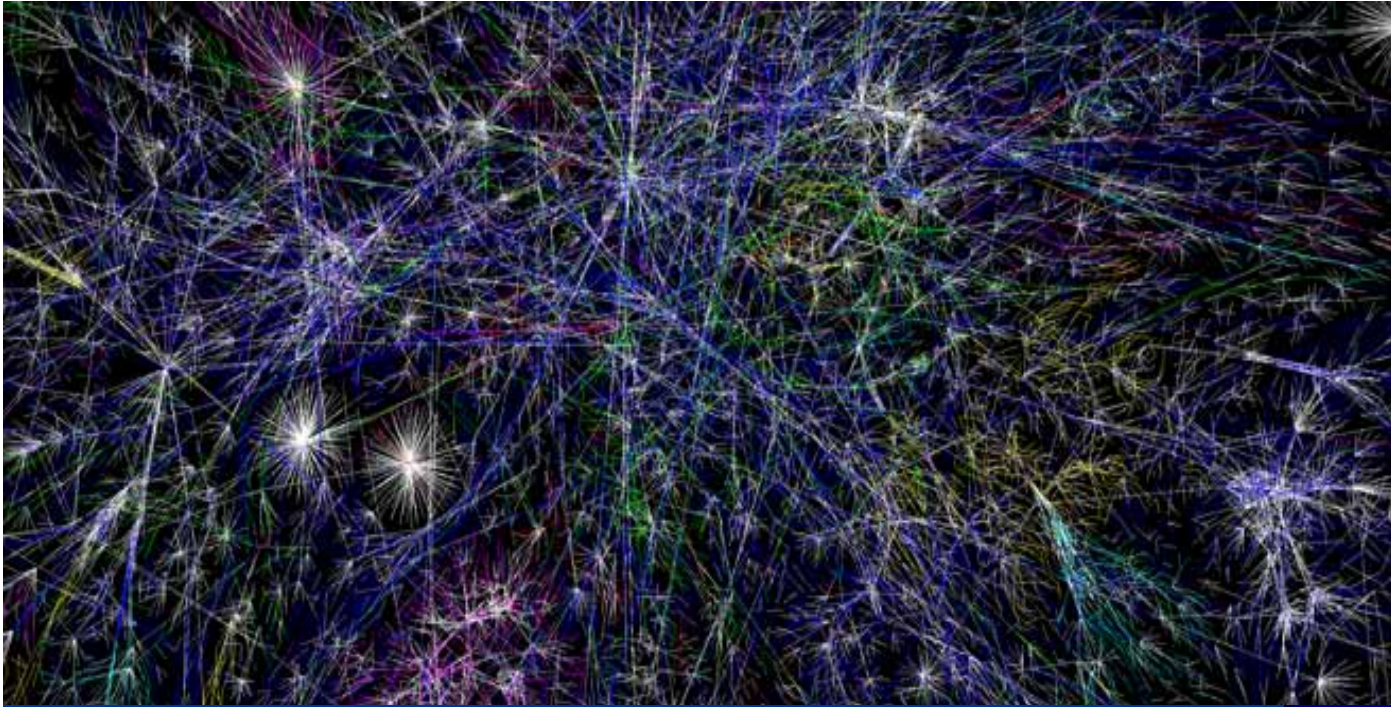
# Nobel Prizes in Electron Devices

- **1956 – The Transistor**  
**William Shockley, John Bardeen, and Walter Brattain**
- **1973 – Tunneling Diode**  
**Leo Esaki, Ivar Giaever**
  - **Josephson Junction**  
**Brian David Josephson**
- **2000 – Integrated Circuit**  
**Jack Kilby**
  - **Semiconductor Heterojunction Devices**  
**Zhores Alferov and Herbert Kroemer**
- **2007 – Giant Magnetoresistive Effect (GMR)**  
**Albert Fert and Peter Grunberg**
- **2009 – Charge Coupled Devices**  
**George Smith and Willard Boyle**
  - **Fiber Optic Technology**  
**Charles Kao**

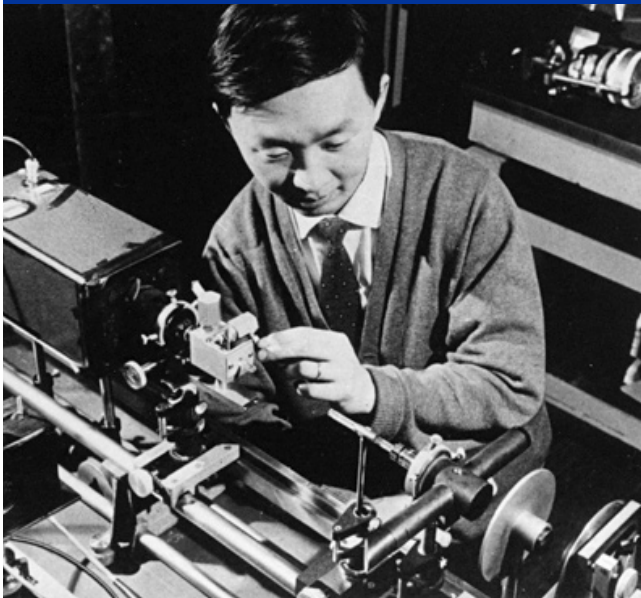


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Global Internet 2009



The Father of  
Fiber Optic  
Communication

By Dr. Lu Terman, at IEDM 2009



By Dr. Lu Terman, at IEDM 2009



**Willard S. Boyle**  
Bell Laboratories  
Murray Hill, NJ, USA



**George E. Smith**  
Bell Laboratories  
Murray Hill, NJ, USA



By Dr. Lu Terman, at IEDM 2009

# *Sir Isaac Newton*

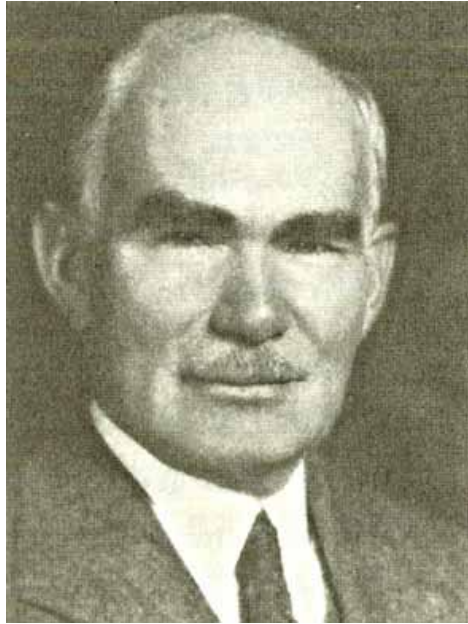
“If I can see so far, it is because I stand on the shoulders of giants”



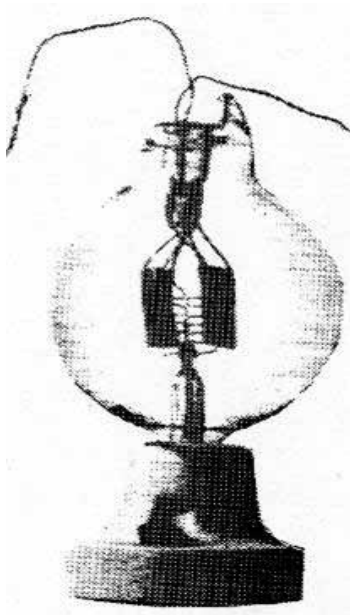
By Dr. Lu Terman, at IEDM 2009

# Importance of Electronics

- There were many inventions in the 20<sup>th</sup> century:  
Airplane, Nuclear Power generation, Computer,  
Space aircraft, etc
- However, everything has to be controlled by  
electronics
- Electronics  
Most important invention in the 20<sup>th</sup> century
- What is Electronics: To use electrons,  
Electronic Circuits

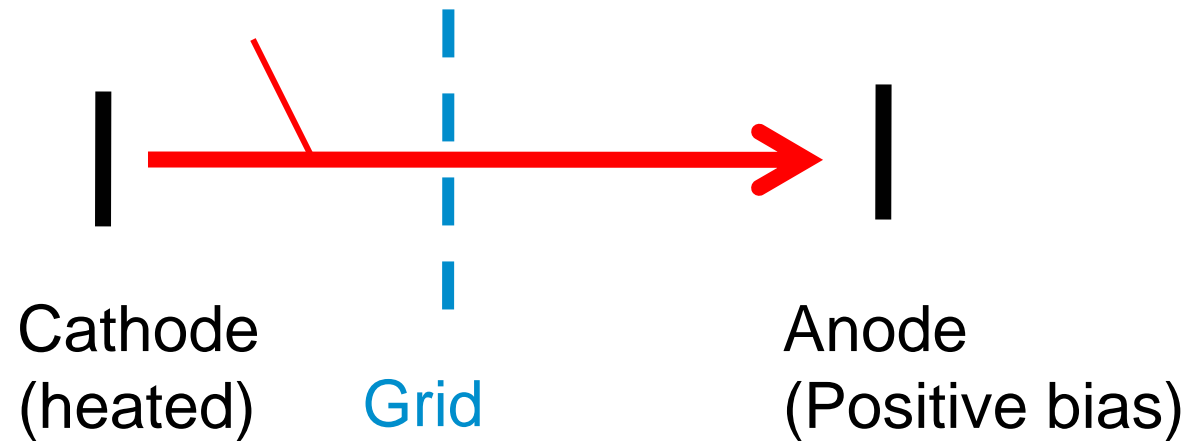


Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

# 4 wives of Lee De Forest

1906 Lucille Sheardown

1907 Nora Blatch

1912 Mary Mayo, singer

1930 Marie Mosquini, silent film actress



Mary

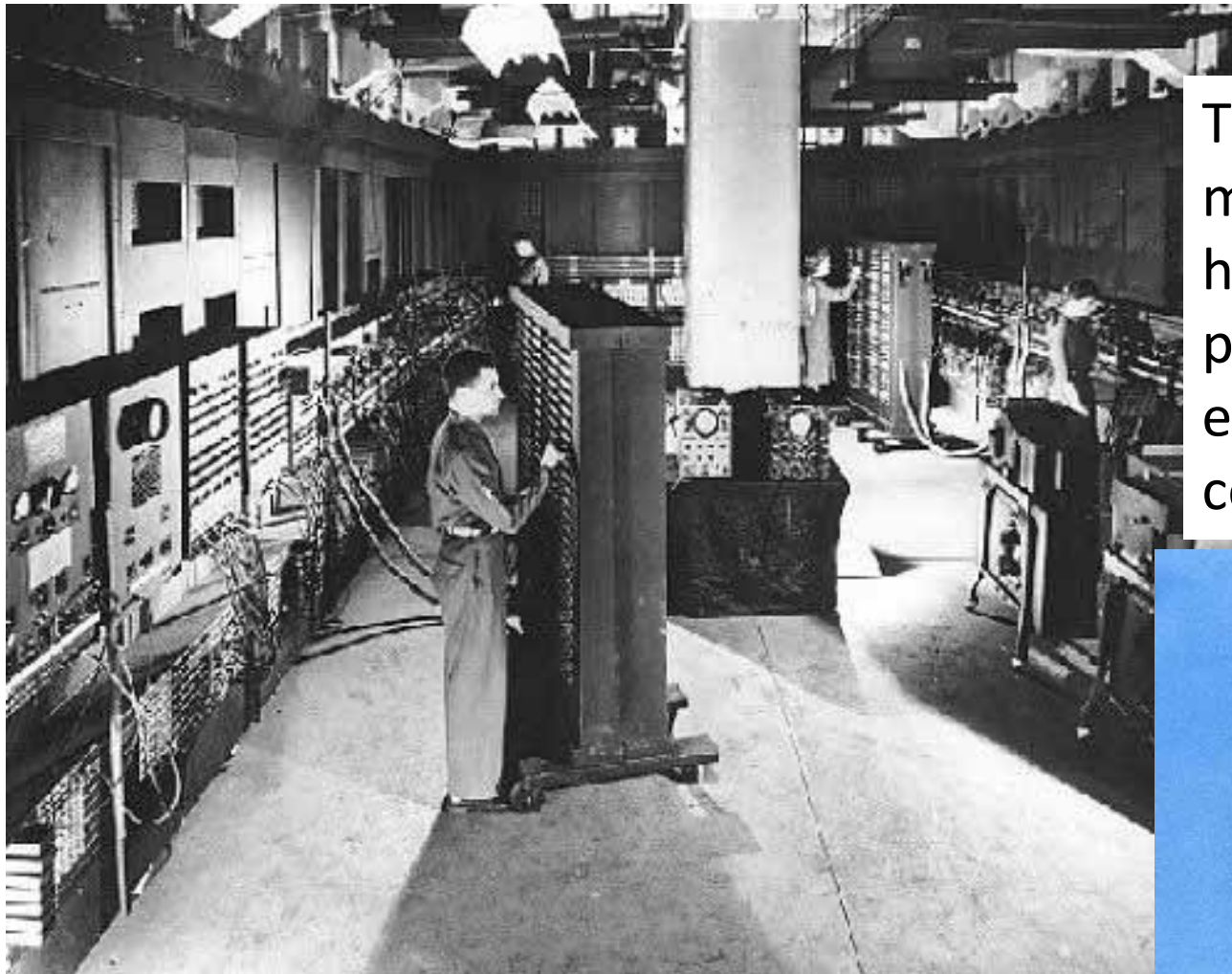


Marie



First Computer Eniac: made of huge number of vacuum tubes 1946  
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device



Today's pocket PC  
made of semiconductor  
has much higher  
performance with  
extremely low power  
consumption

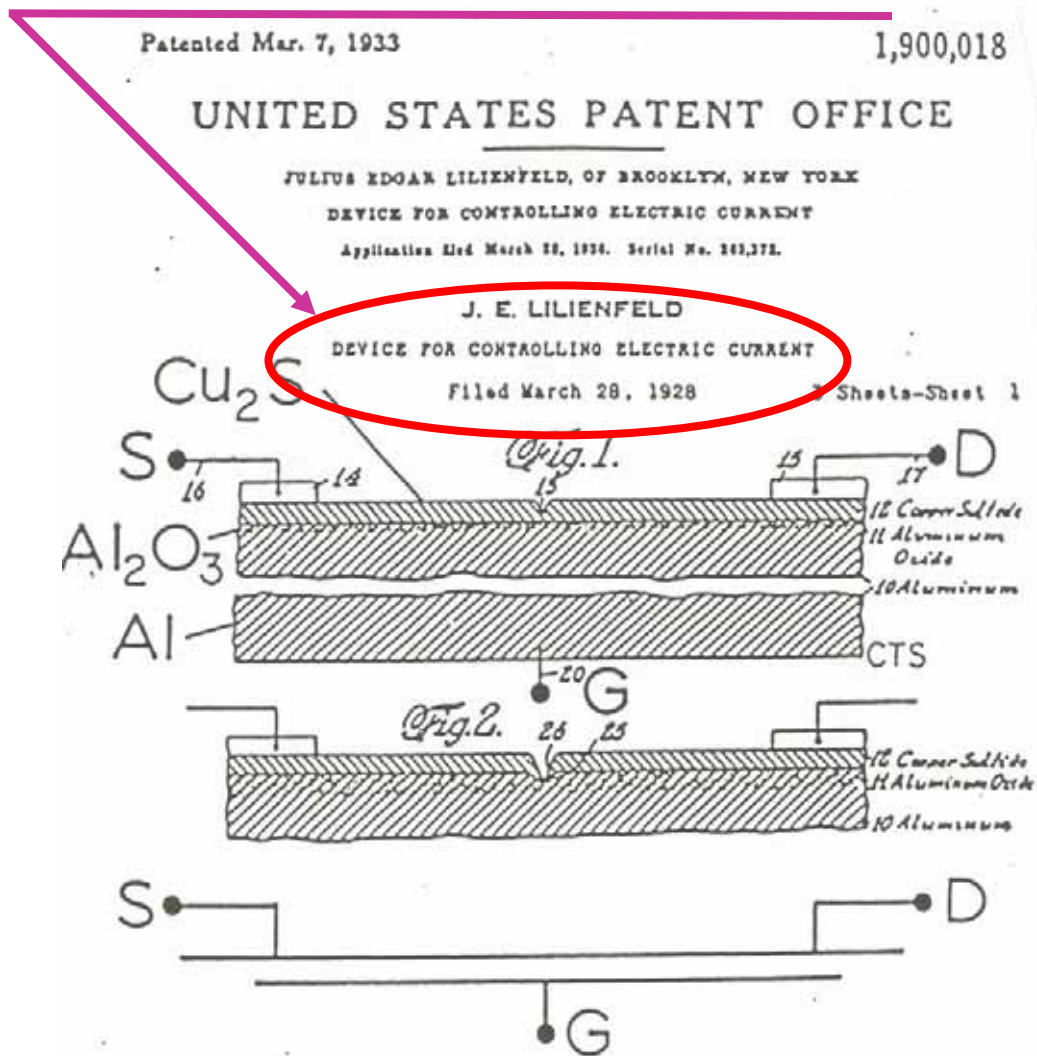




# J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

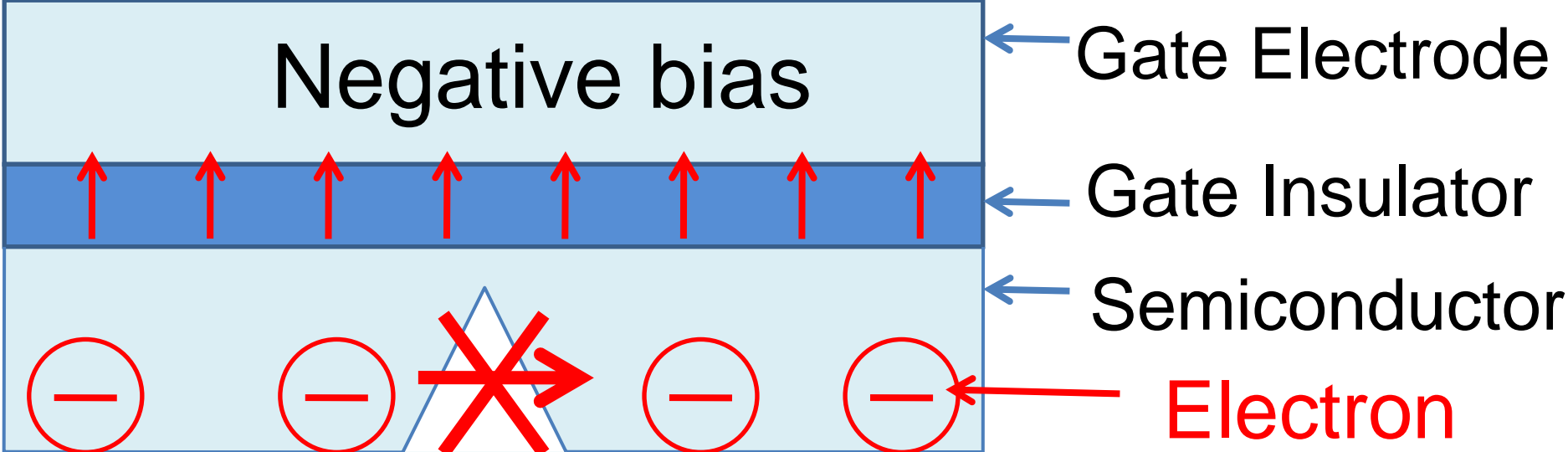
Filed March 28, 1928



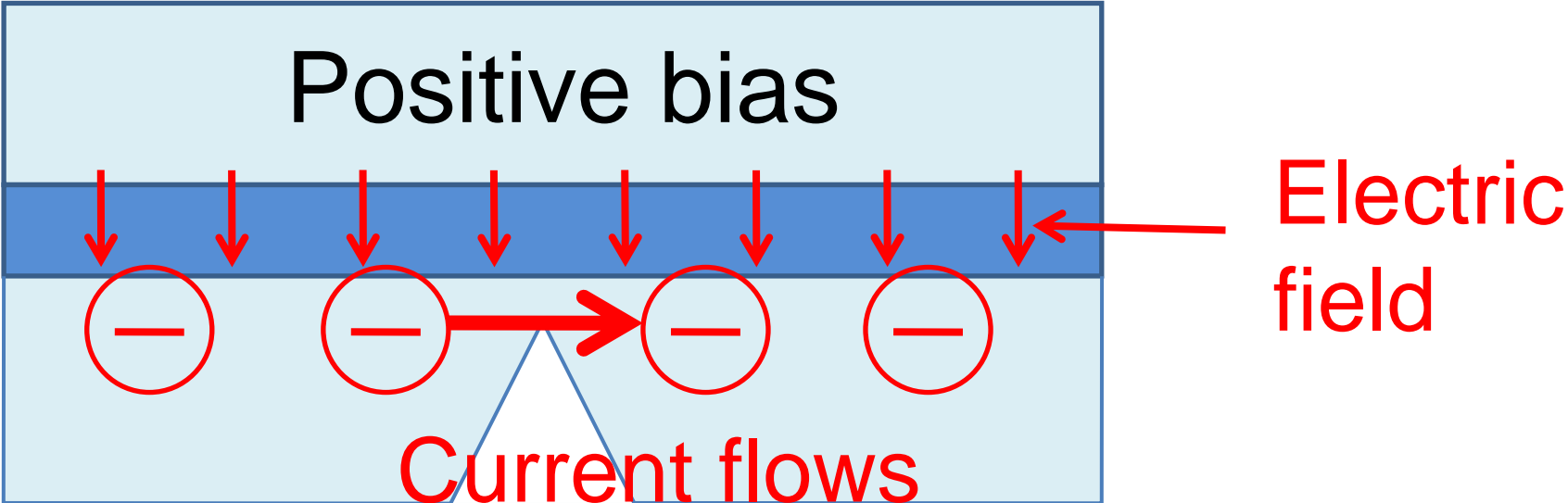
## J.E.LILIENFELD



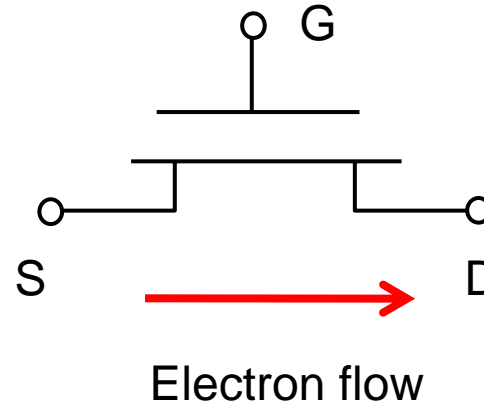
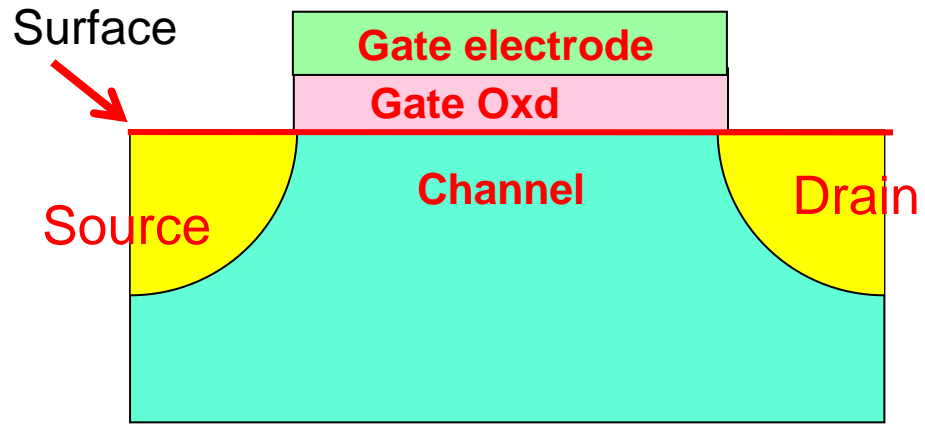
# Capacitor structure with notch



No current



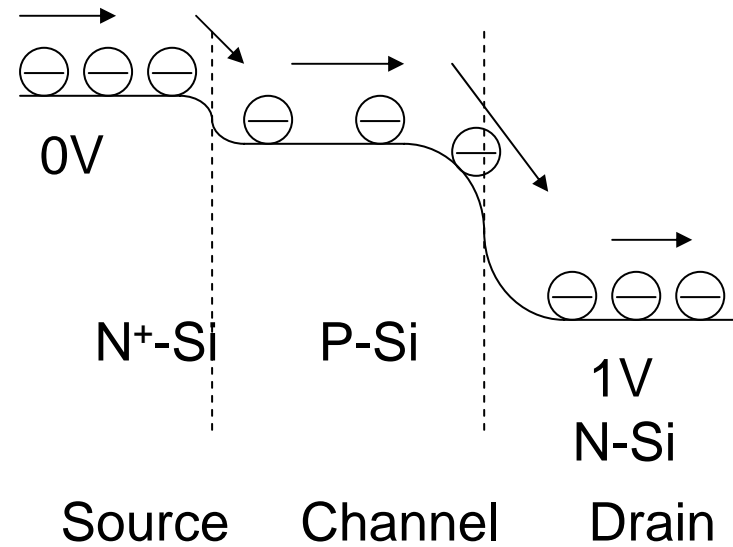
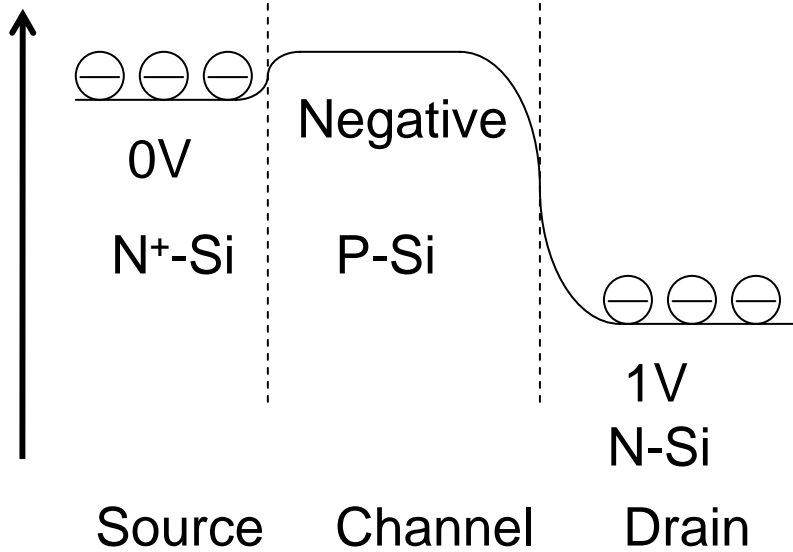
Current flows



0 bias for gate

Positive bias for gate

Surface Potential (Negative direction)

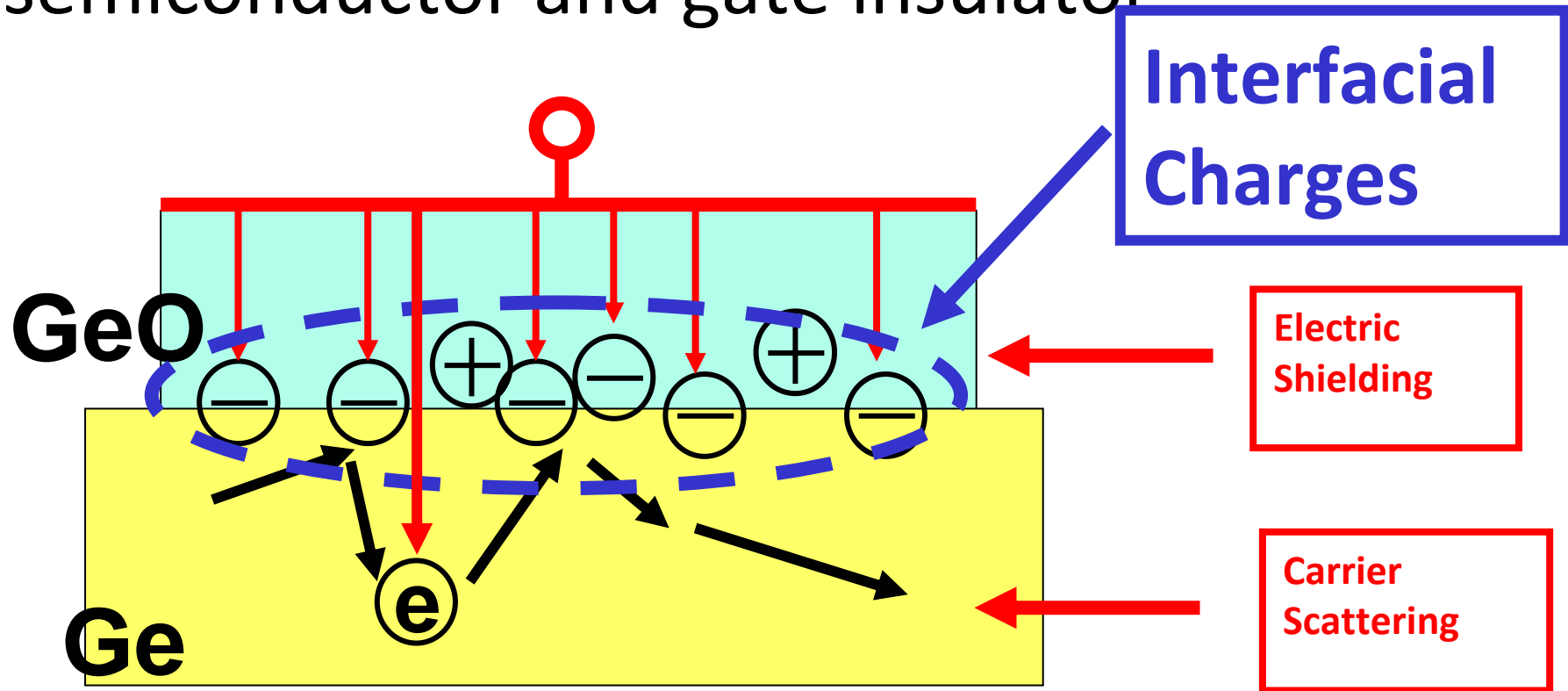


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator



Drain Current was several orders of magnitude smaller than expected

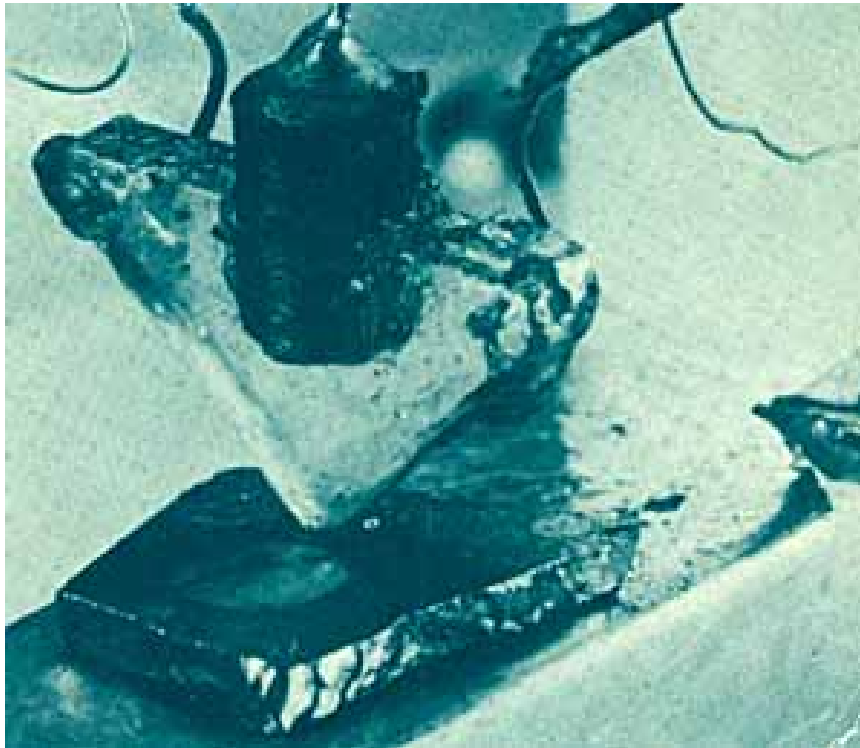
Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.

This is the 1<sup>st</sup> Transistor:

**Not Field Effect Transistor,  
But Bipolar Transistor (another mechanism)**

## 1947: 1<sup>st</sup> transistor



**Bipolar using Ge**

J. Bardeen

W. Bratten,

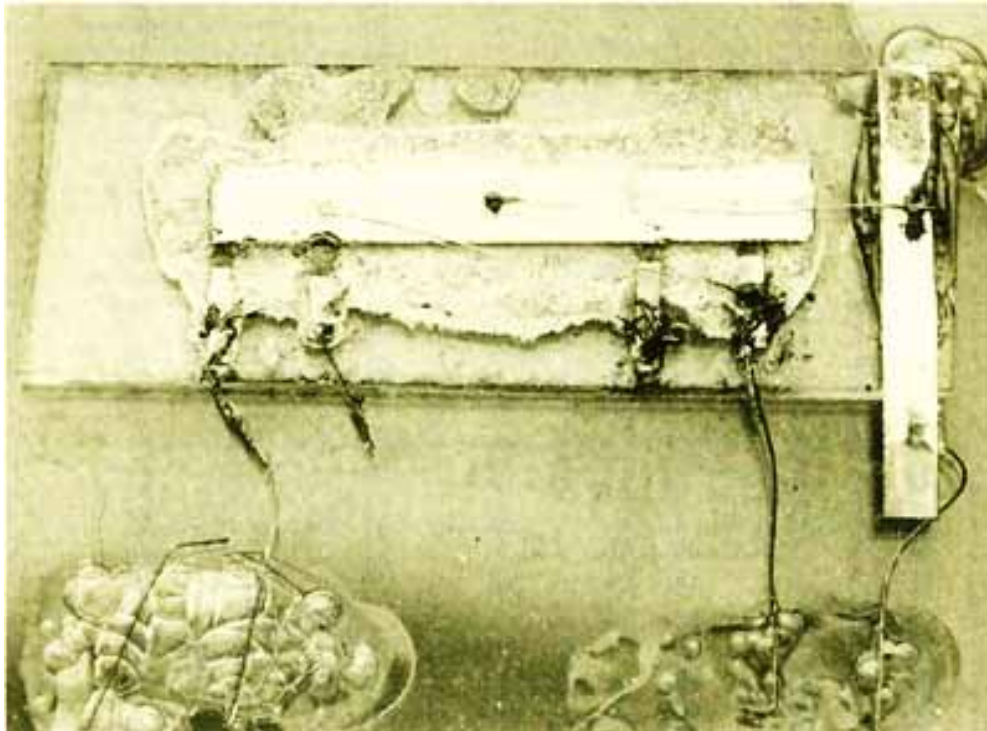


W. Shockley

## 1958: 1st Integrated Circuit

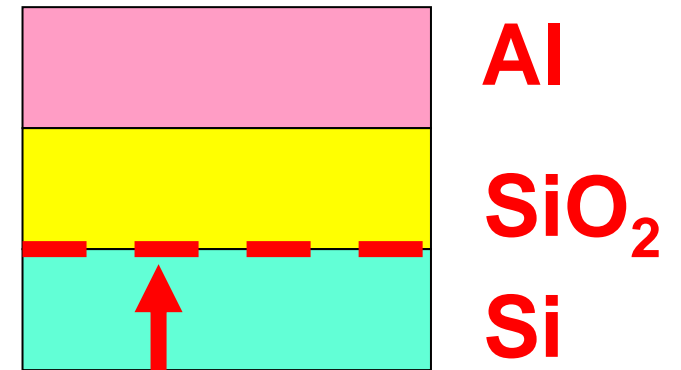
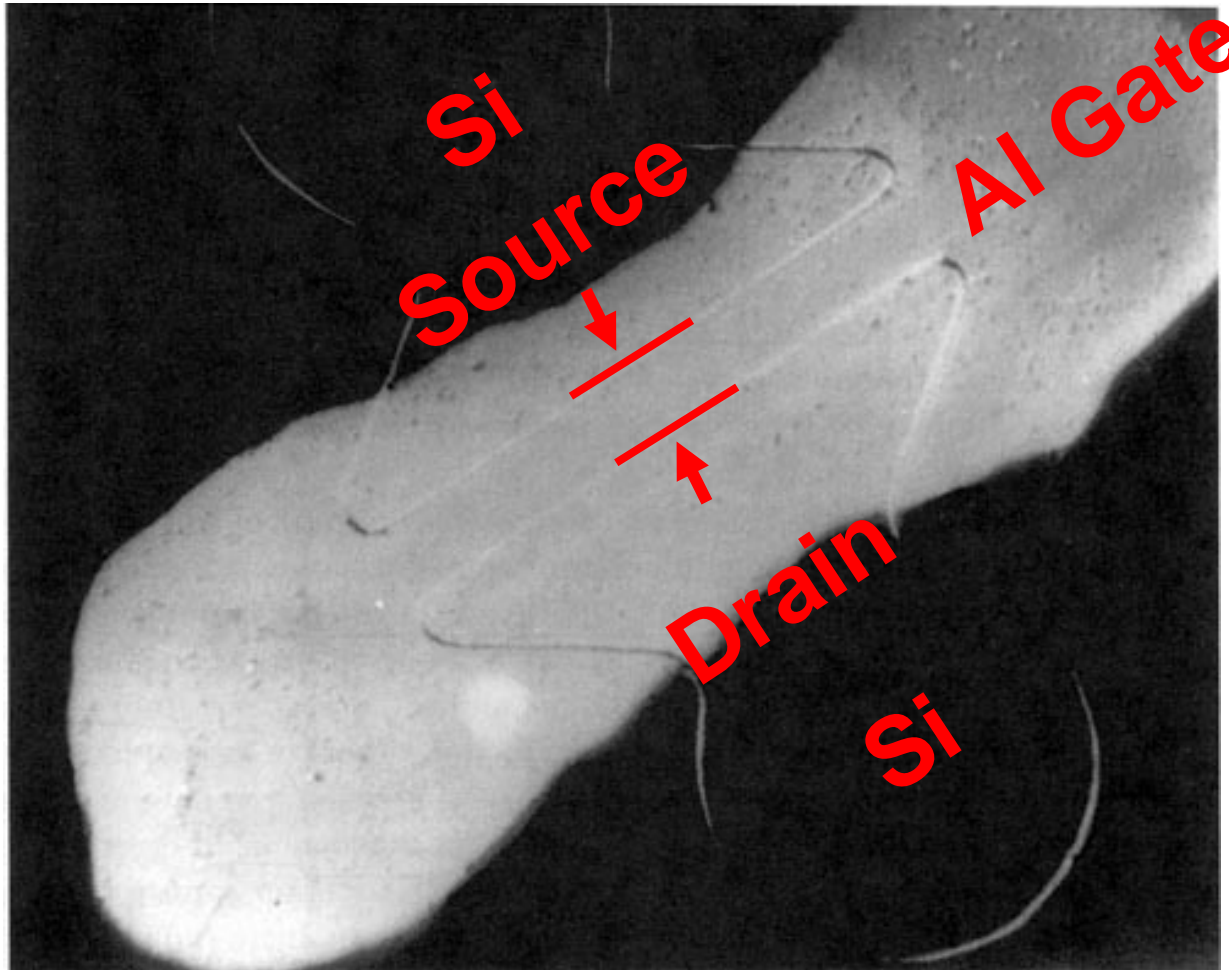
Jack S. Kilby

Connect 2 bipolar transistors in the Same substrate by bonding wire.



**1960:** First MOSFET  
by D. Kahng and M. Atalla

**Top View**

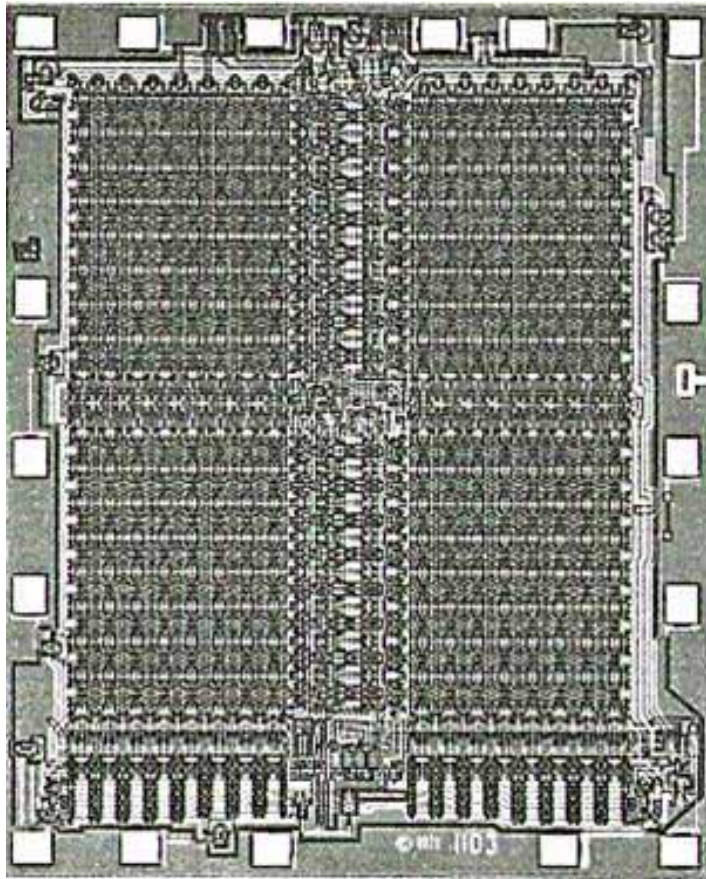


Si/SiO<sub>2</sub> Interface is  
extraordinarily good

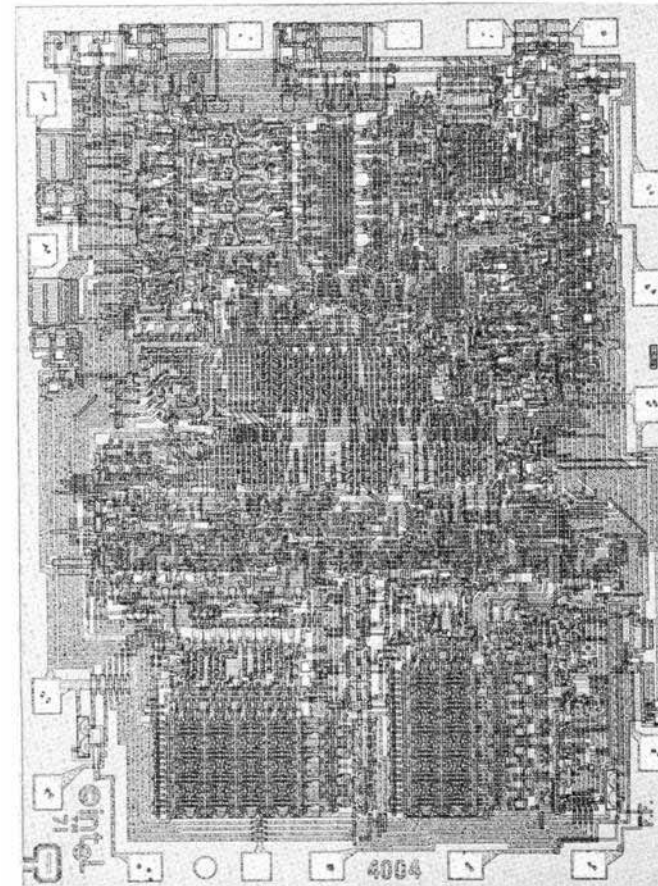


# 1970,71: 1st generation of LSIs

**DRAM Intel 1103**



**MPU Intel 4004**



MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000 <sup>34</sup>

Gate Electrode  
Poly Si

Gate Insulator  
SiO<sub>2</sub>

Substrate  
Si

**MOSFET:** Metal Oxide Semiconductor  
Field Effect Transistor

**Use Gate Field Effect for switching**

Gate Electrode  
Poly Si

Gate Insulator  
SiO<sub>2</sub>

Source

n-Si



n-Si

Drain

p-Si

Si

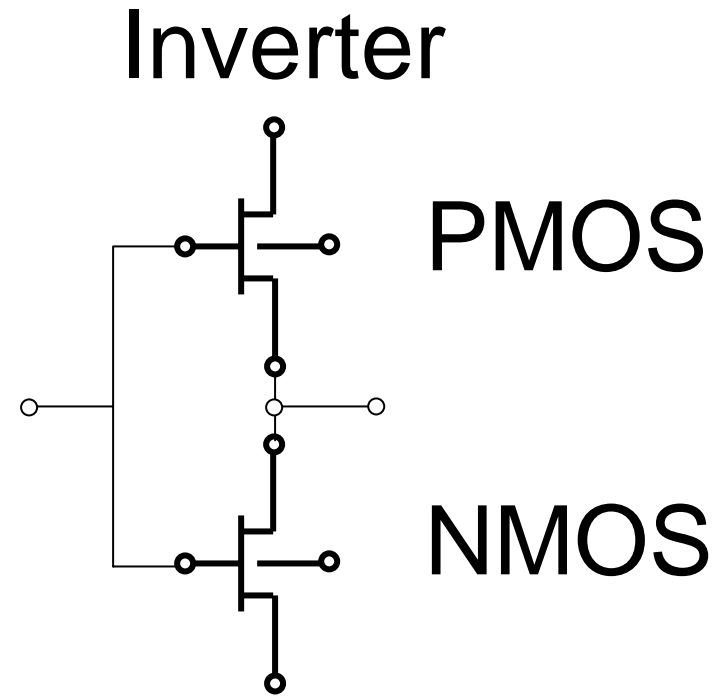
Substrate

Channel

N-MOS (N-type MOSFET)

# CMOS

Complimentary MOS



When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

Needless to say, but....

CMOS Technology:

Indispensable for our human society

All the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and  
world economical activities immediately stop.

Cellarer phone dose not exists

# Downsizing of the components has been the driving force for circuit evolution



1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 $\mu$ m	100 nm
$10^{-1}$ m	$10^{-2}$ m	$10^{-3}$ m	$10^{-5}$ m	$10^{-7}$ m

In 100 years, the size reduced by one million times. There have been many devices from stone age. **We have never experienced such a tremendous reduction of devices in human history.**

## Downsizing

### 1. Reduce Capacitance

→ Reduce switching time of MOSFETs

→ Increase clock frequency

→ Increase circuit operation speed

### 2. Increase number of Transistors

→ Parallel processing

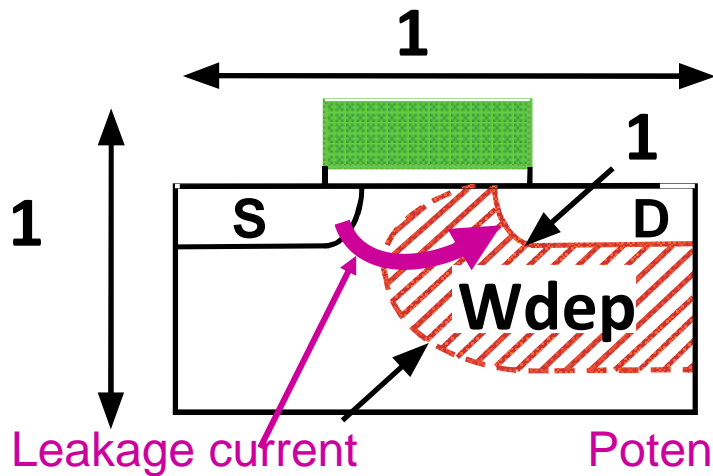
→ Increase circuit operation speed

---

Downsizing contribute to the performance increase in double ways

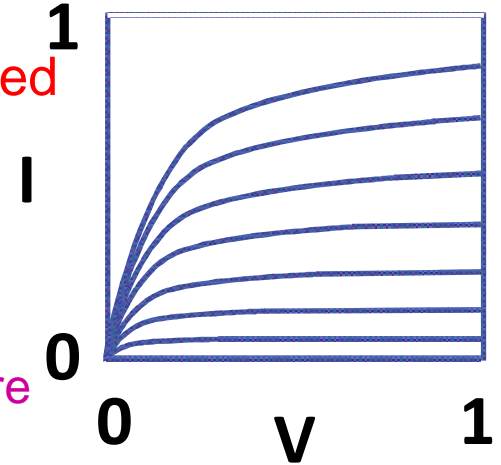
**Thus, downsizing of Si devices is the most important and critical issue.**

Scaling Method: by R. Dennard in 1974



**Wdep:** Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed  
Otherwise, large leakage  
between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

**K=0.7  
for  
example**

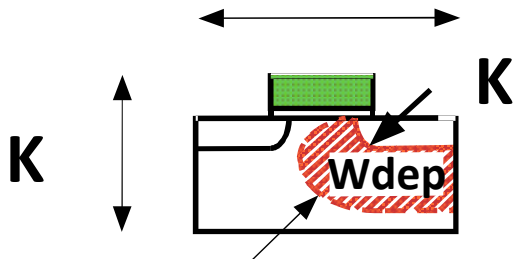


**X , Y , Z : K,    V : K,    Na : 1/K**

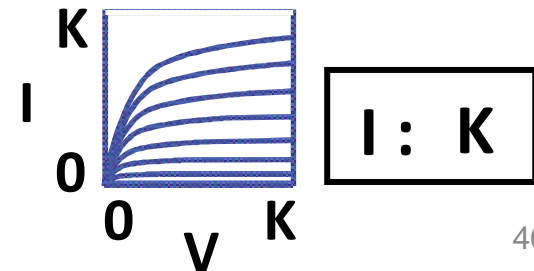
By the scaling, Wdep is suppressed in proportion,  
and thus, leakage can be suppressed.

**K**

→ Good scaled I-V characteristics



**Wdep ∝ √(V/Na)  
: K**



**I : K**



## Downscaling merit: Beautiful!

Geometry & Supply voltage	$L_g, W_g$ $T_{ox}, V_{dd}$	K	<b>Scaling K : K=0.7 for example</b>
Drive current in saturation	$I_d$	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ $C_o$ : gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
$I_d$ per unit $W_g$	$I_d/\mu m$	1	$I_d$ per unit $W_g = I_d / W_g = 1$
Gate capacitance	$C_g$	K	$C_g = \epsilon_o \epsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	$\tau$	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	$A_{chip}$	$\alpha$	<b><math>\alpha</math>: Scaling factor <math>\rightarrow</math> In the past, <math>\alpha &gt; 1</math> for most cases</b>
Integration (# of Tr)	N	$\alpha/K^2$	$N \rightarrow \alpha/K^2 = 1/K^2$ , when $\alpha=1$
Power per chip	P	$\alpha$	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha = 1$ , when $\alpha=1$

$k = 0.7$  and  $\alpha = 1$

Single MOFET

$V_{dd} \rightarrow 0.7$

$L_g \rightarrow 0.7$

$I_d \rightarrow 0.7$

$C_g \rightarrow 0.7$

$P$  (Power)/Clock

$\rightarrow 0.7^3 = 0.34$

$\tau$  (Switching time)  $\rightarrow 0.7$

$k = 0.7^2 = 0.5$  and  $\alpha = 1$

$V_{dd} \rightarrow 0.5$

$L_g \rightarrow 0.5$

$I_d \rightarrow 0.5$

$C_g \rightarrow 0.5$

$P$  (Power)/Clock

$\rightarrow 0.5^3 = 0.125$

$\tau$  (Switching time)  $\rightarrow 0.5$

Chip

$N$  (# of Tr)  $\rightarrow 1/0.7^2 = 2$

$f$  (Clock)  $\rightarrow 1/0.7 = 1.4$

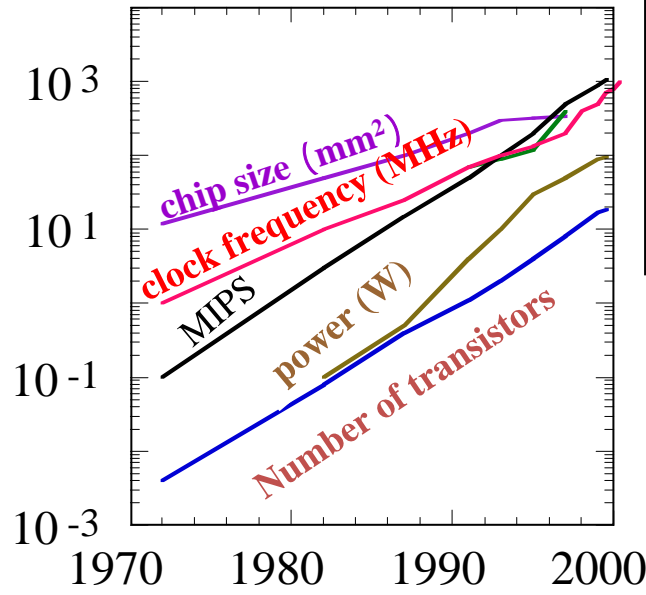
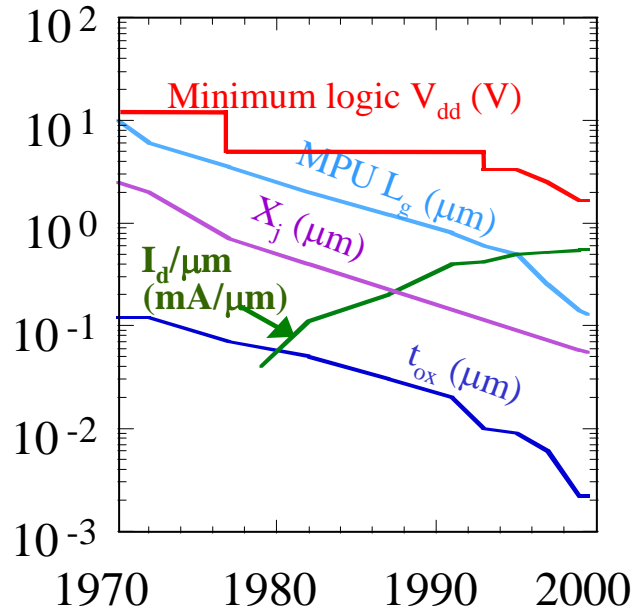
$P$  (Power)  $\rightarrow 1$

$N$  (# of Tr)  $\rightarrow 1/0.5^2 = 4$

$f$  (Clock)  $\rightarrow 1/0.5 = 2$

$P$  (Power)  $\rightarrow 1$

# Actual past downscaling trend until year 2000



Past 30 years scaling  
 Merit: N, f increase  
 Demerit: P increase

$V_{dd}$  scaling insufficient  
 ↓  
 Additional significant increase in  $I_d, f, P$

Source: Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

## Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
$L_g$	K	$10^{-2}$	$I_d$	K ( $10^{-2}$ )	$10^{-1}$	f	$1/K(10^2)$	$10^3$
$t_{ox}$	K( $10^{-2}$ )	$10^{-2}$	$I_d/\mu m$	1	$10^1$	P	$\alpha(10^1)$	$10^5$
$V_{dd}$	K( $10^{-2}$ )	$10^{-1}$	N	$\alpha/K^2(10^5)$	$10^4$	= $f\alpha NCV^2$		
$A_{chip}$	$\alpha$	$10^1$						

$V_d$  scaling insufficient,  $\alpha$  increased → N,  $I_d$ , f, P increased significantly

# Many people wanted to say about the limit. Past predictions were not correct!!

---

Period	Expected limit(size)	Cause
Late 1970's	1 $\mu$ m:	SCE
Early 1980's	0.5 $\mu$ m:	S/D resistance
Early 1980's	0.25 $\mu$ m:	Direct-tunneling of gate SiO <sub>2</sub>
Late 1980's	0.1 $\mu$ m:	'0.1 $\mu$ m brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

**VLSI text book written 1979 predict that 0.25 micrometer would be the limit because of direct-tunneling current through the very thin-gate oxide.**

# INTRODUCTION TO **VLSI** SYSTEMS

CARVER MEAD • LYNN CONWAY





C. Mead

L. Conway

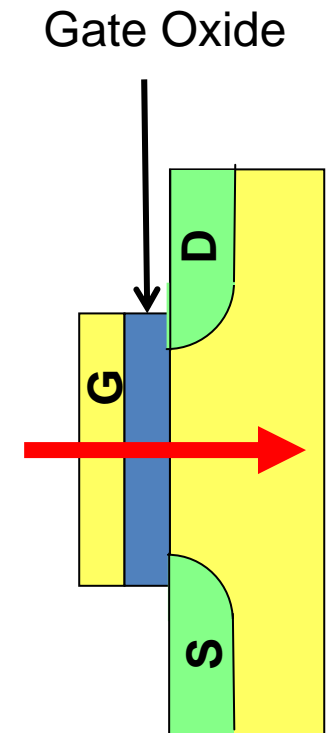
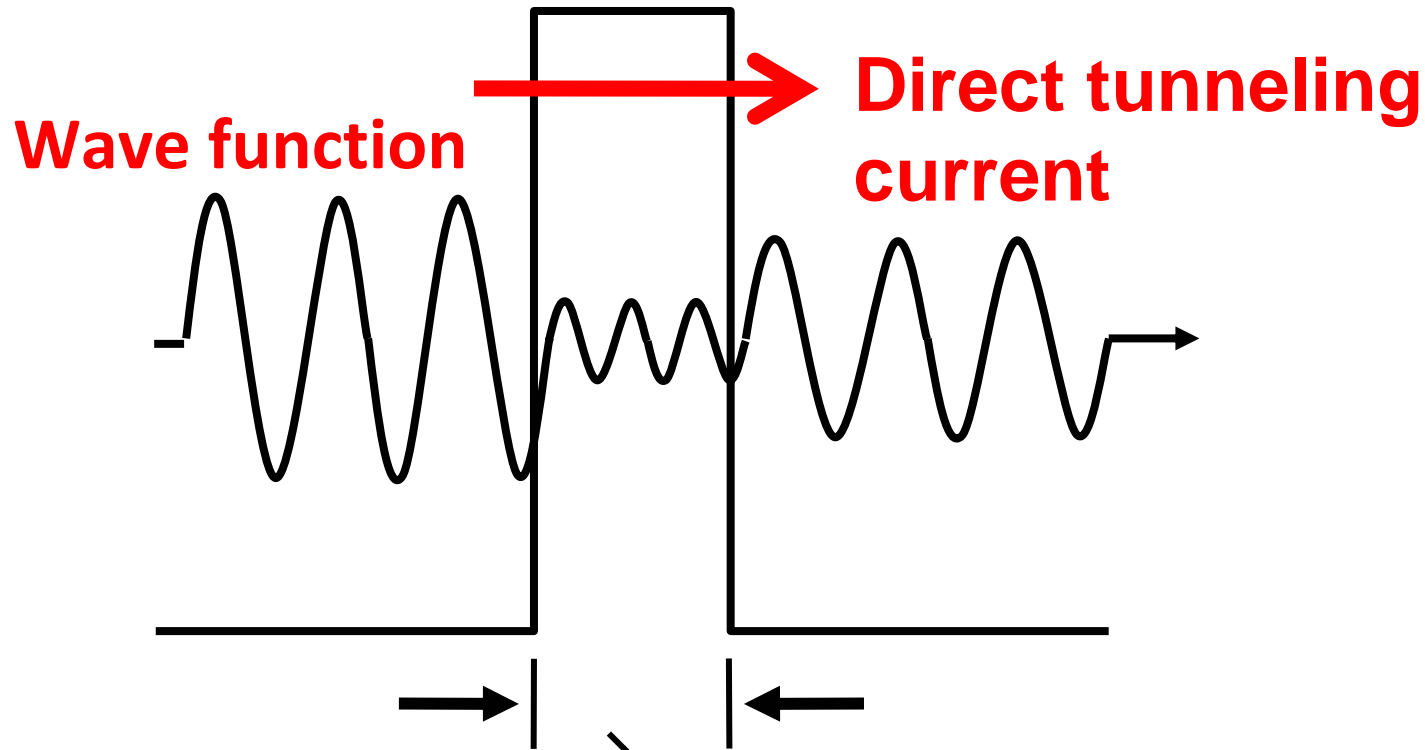
## VLSI textbook

**Finally, there appears to be a fundamental limit <sup>10</sup> of approximately quarter micron channel length, where certain physical effects such as the **tunneling through the gate oxide** ..... begin to make the devices of smaller dimension unworkable.**

# Direct-tunneling effect

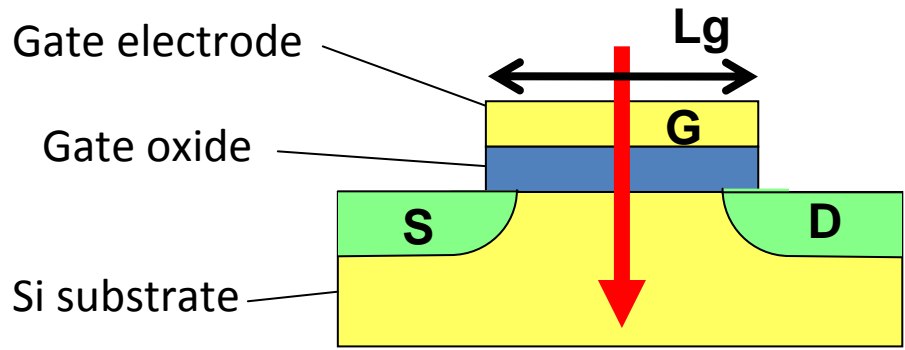
Gate Electrode      Gate Oxide      Si Substrate

**Potential Barrier**



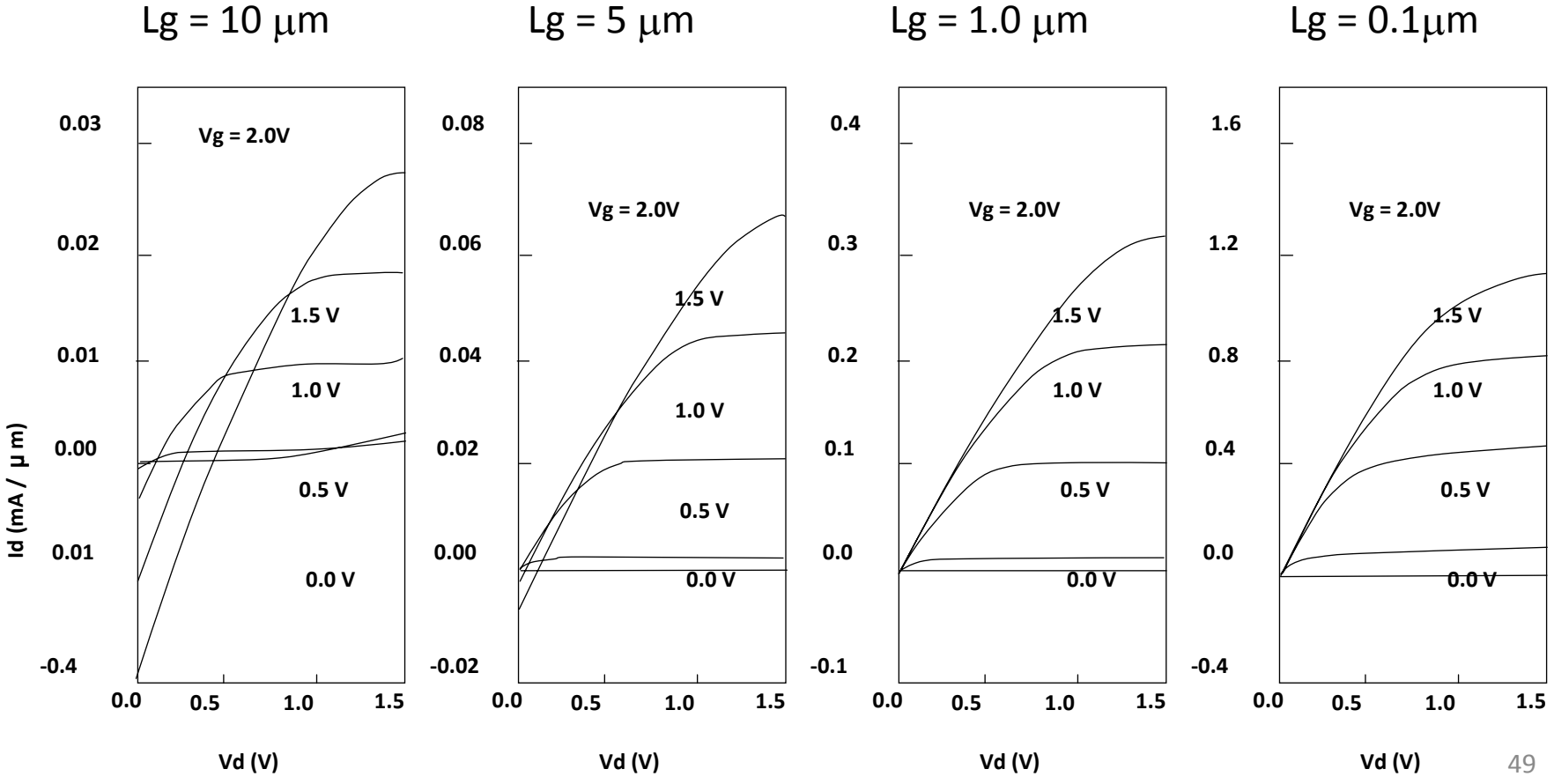
**Direct tunneling leakage current start to flow when the thickness is 3 nm.**

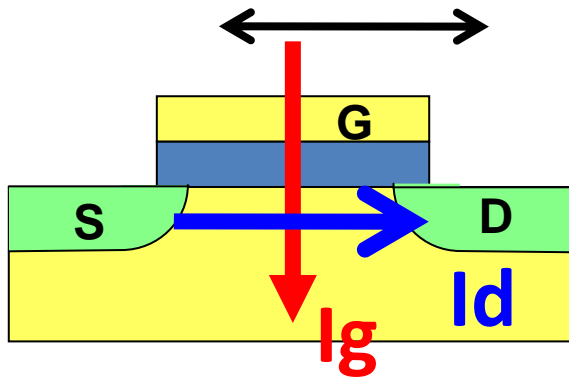




**Direct tunneling leakage was found to be OK! In 1994!**

MOSFETs with 1.5 nm gate oxide





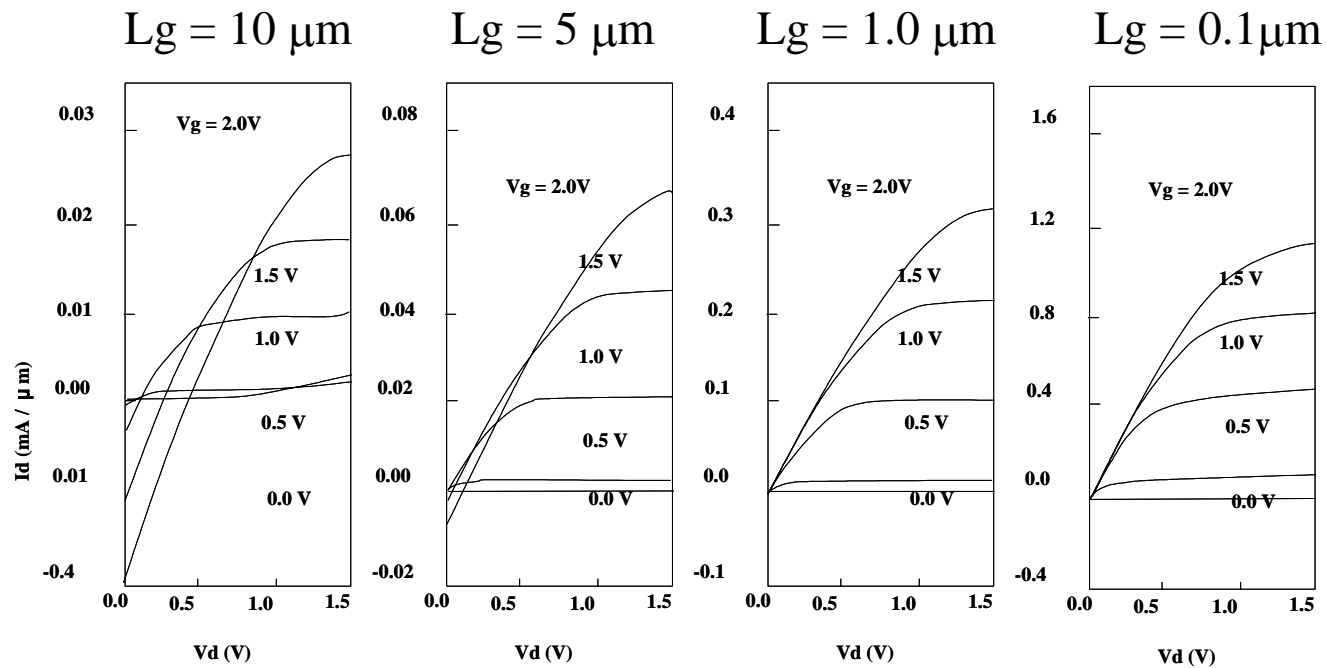
Gate leakage:  $I_g \propto \text{Gate Area} \propto \text{Gate length (L}_g)$

Drain current:  $I_d \propto 1/\text{Gate length (L}_g)$

$L_g \rightarrow$  small,

Then,  $I_g \rightarrow$  small,  $I_d \rightarrow$  large, Thus,  $I_g/I_d \rightarrow$  very small

$I_d$



**Do not believe a text book statement, blindly!**

**Never Give Up!**

**No one knows future!**

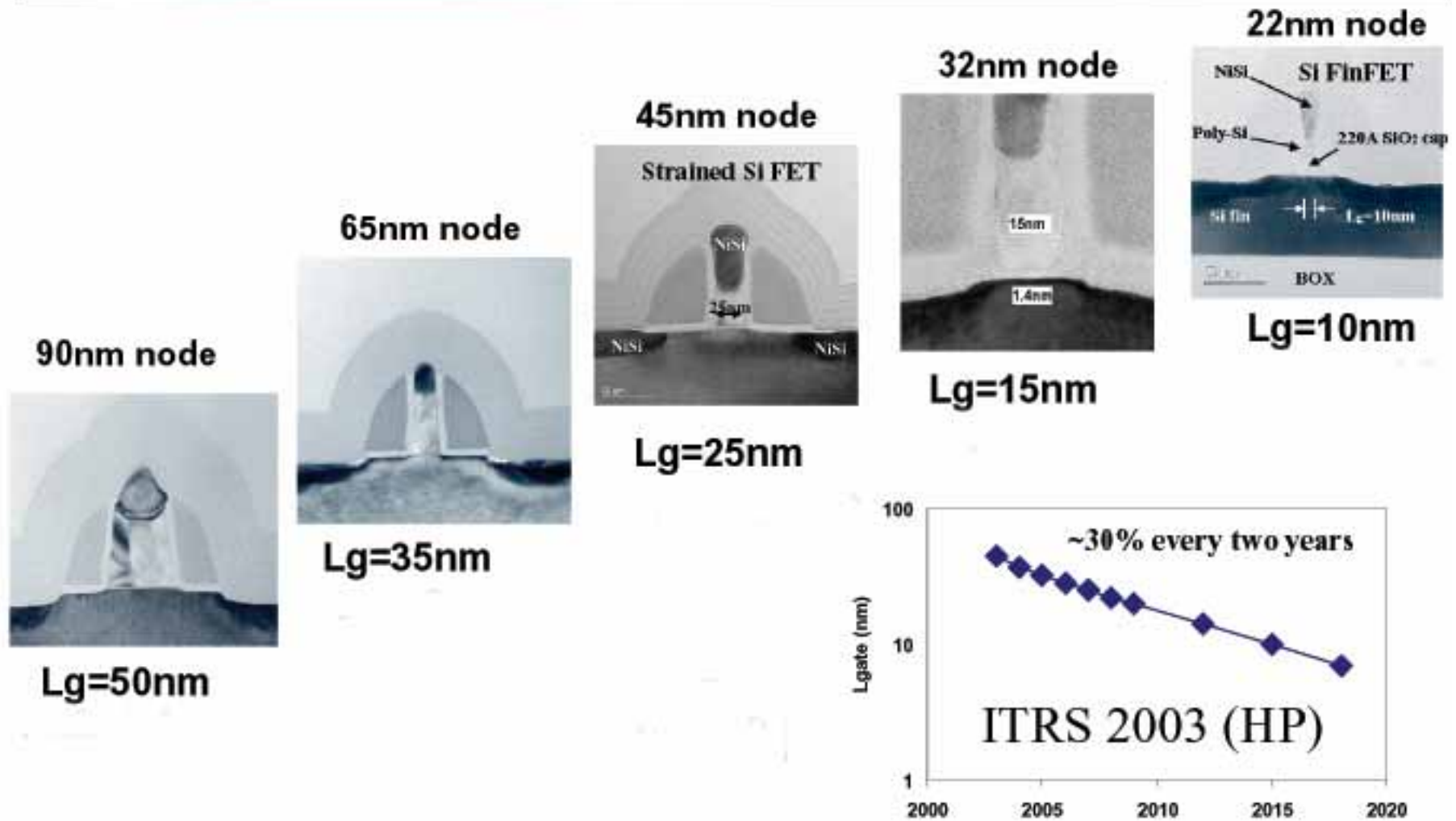
**There would be a solution!**

**Think, Think, and Think!**

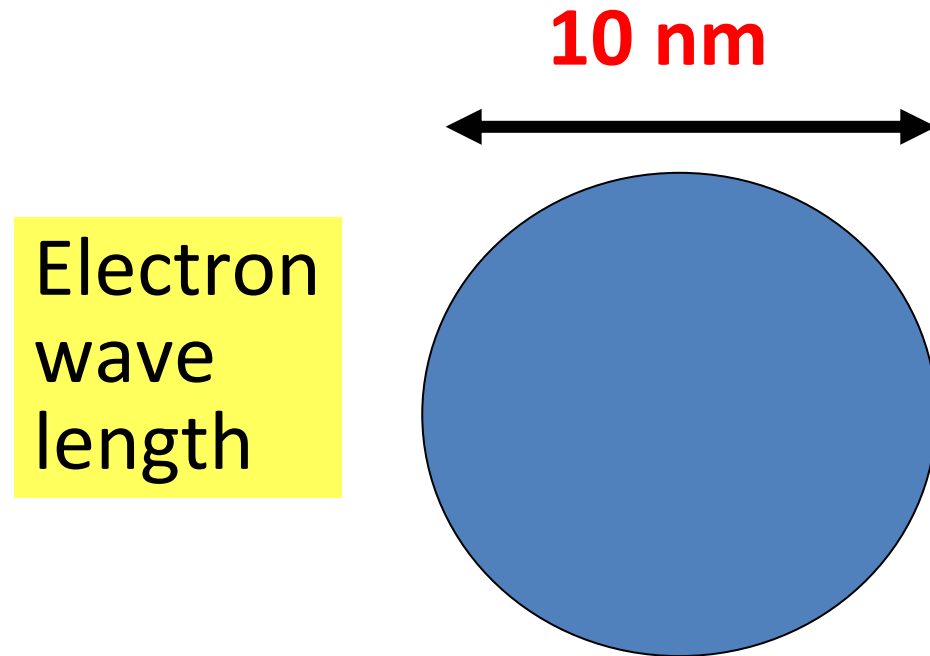
**Or, Wait the time!**

**Some one will think for you**

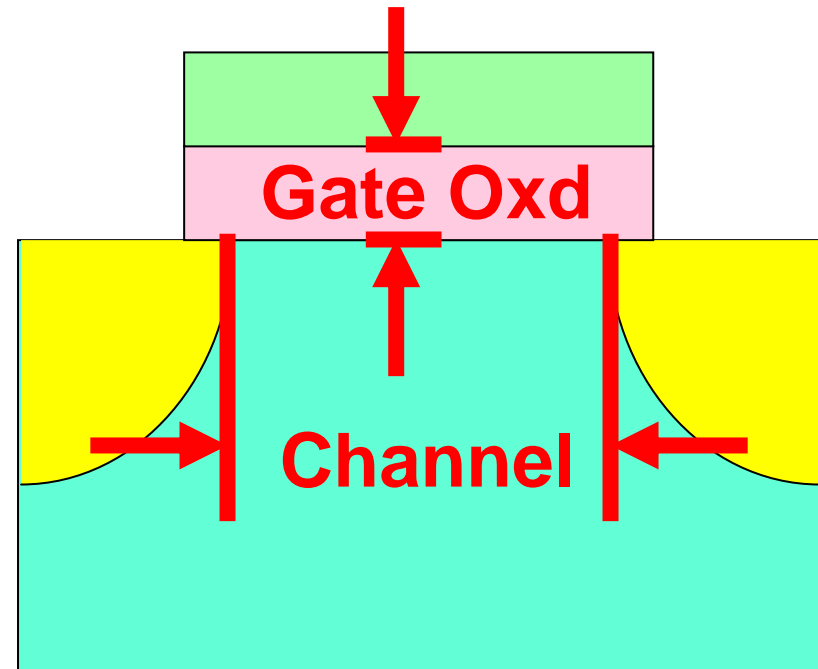
# Transistor Scaling Continues



# Downsizing limit?

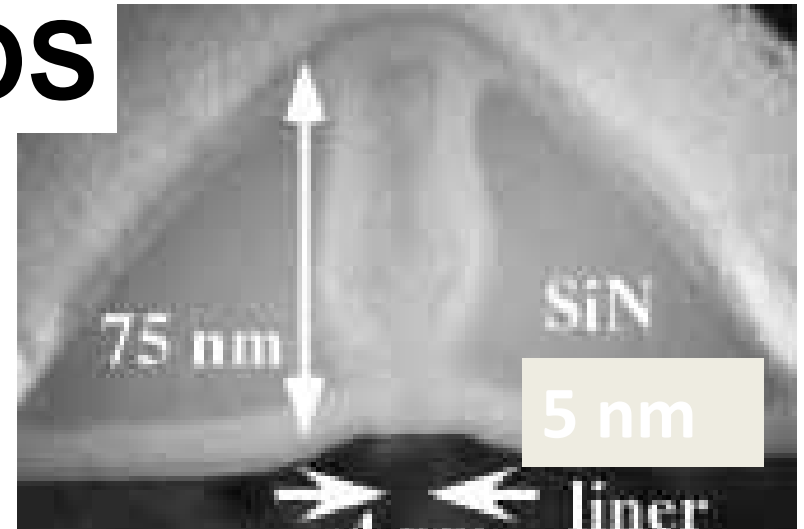


# Channel length?

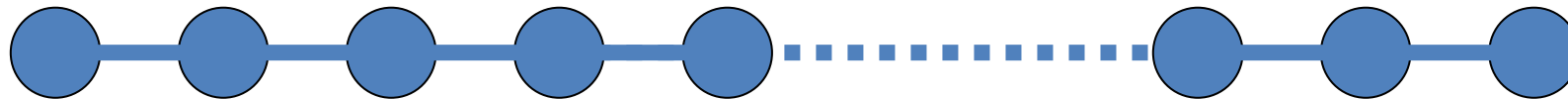


# 5 nm gate length CMOS

## Is a Real Nano Device!!

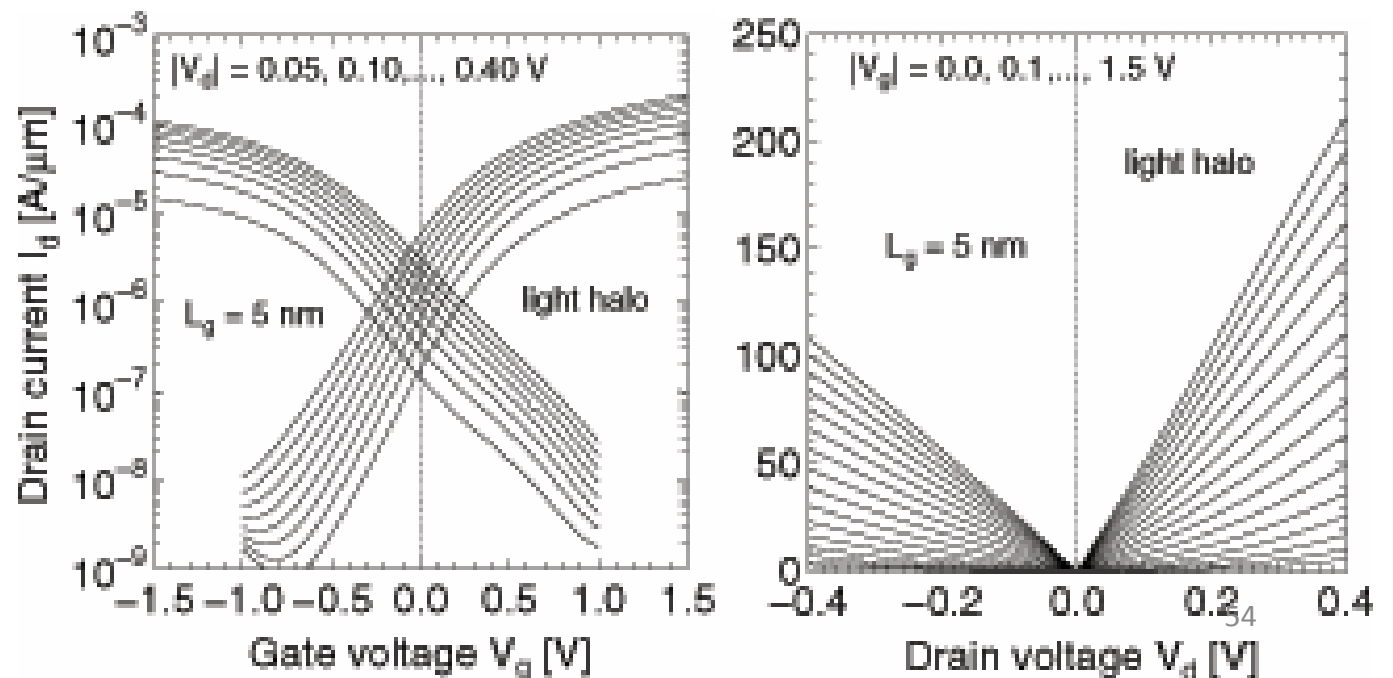


*Length of 18 Si atoms*



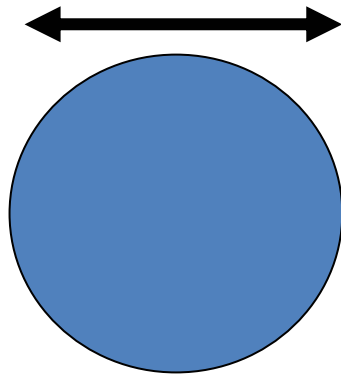
H. Wakabayashi  
et.al, NEC

IEDM, 2003



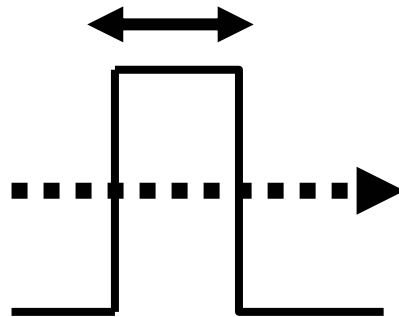
Electron  
wave  
length

**10 nm**



Tunneling  
distance

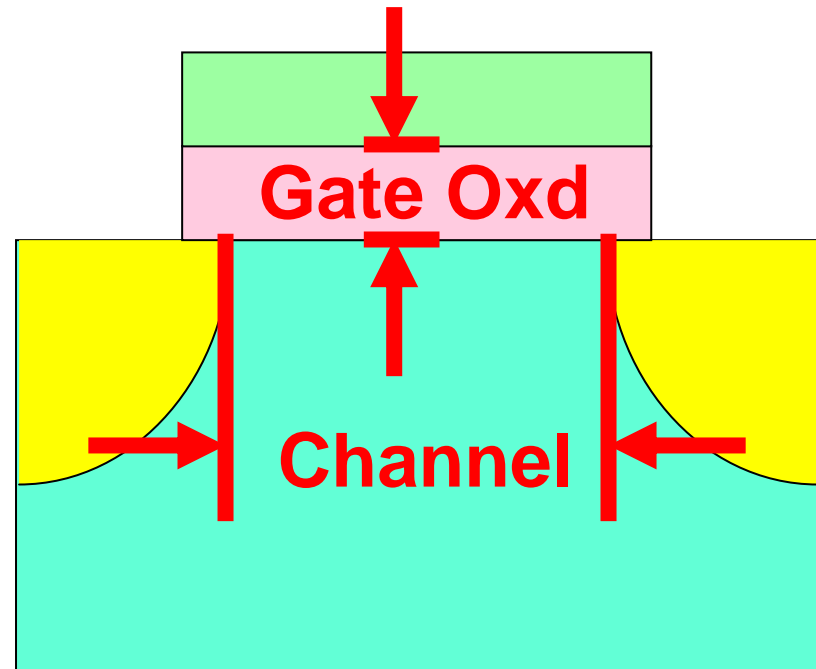
**3 nm**



Downsizing limit!

Channel length

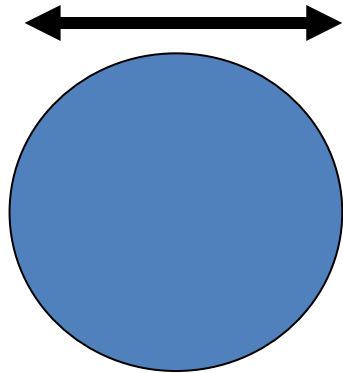
Gate oxide thickness



**Prediction now!**

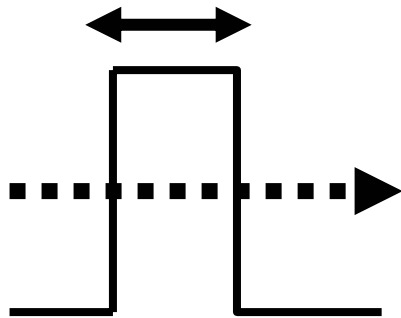
Electron  
wave  
length

**10 nm**



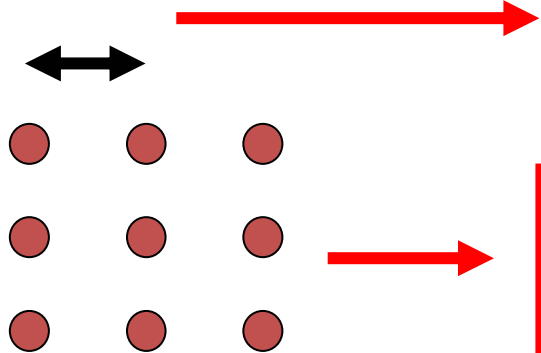
Tunneling  
distance

**3 nm**



Atom  
distance

**0.3 nm**



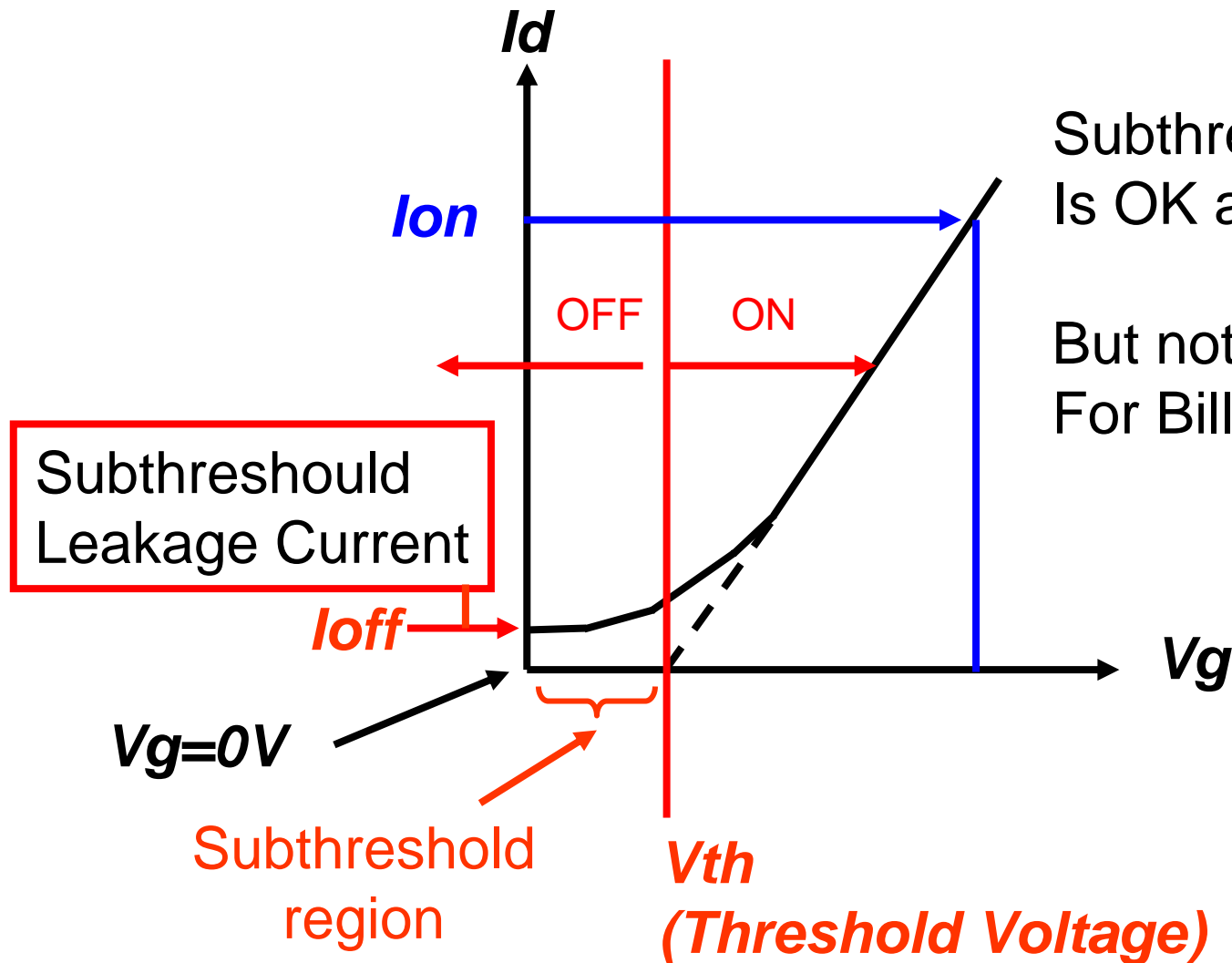
MOSFET operation

**$L_g = 2 \sim 1.5 \text{ nm?}$**

**Below this,  
no one knows future!**



# Subthreshold leakage current of MOSFET



Subthreshold Current  
Is OK at Single Tr. level

But not OK  
For Billions of Trs.

**Vth cannot be decreased anymore**

Log scale Id plot

**significant Ioff increase**

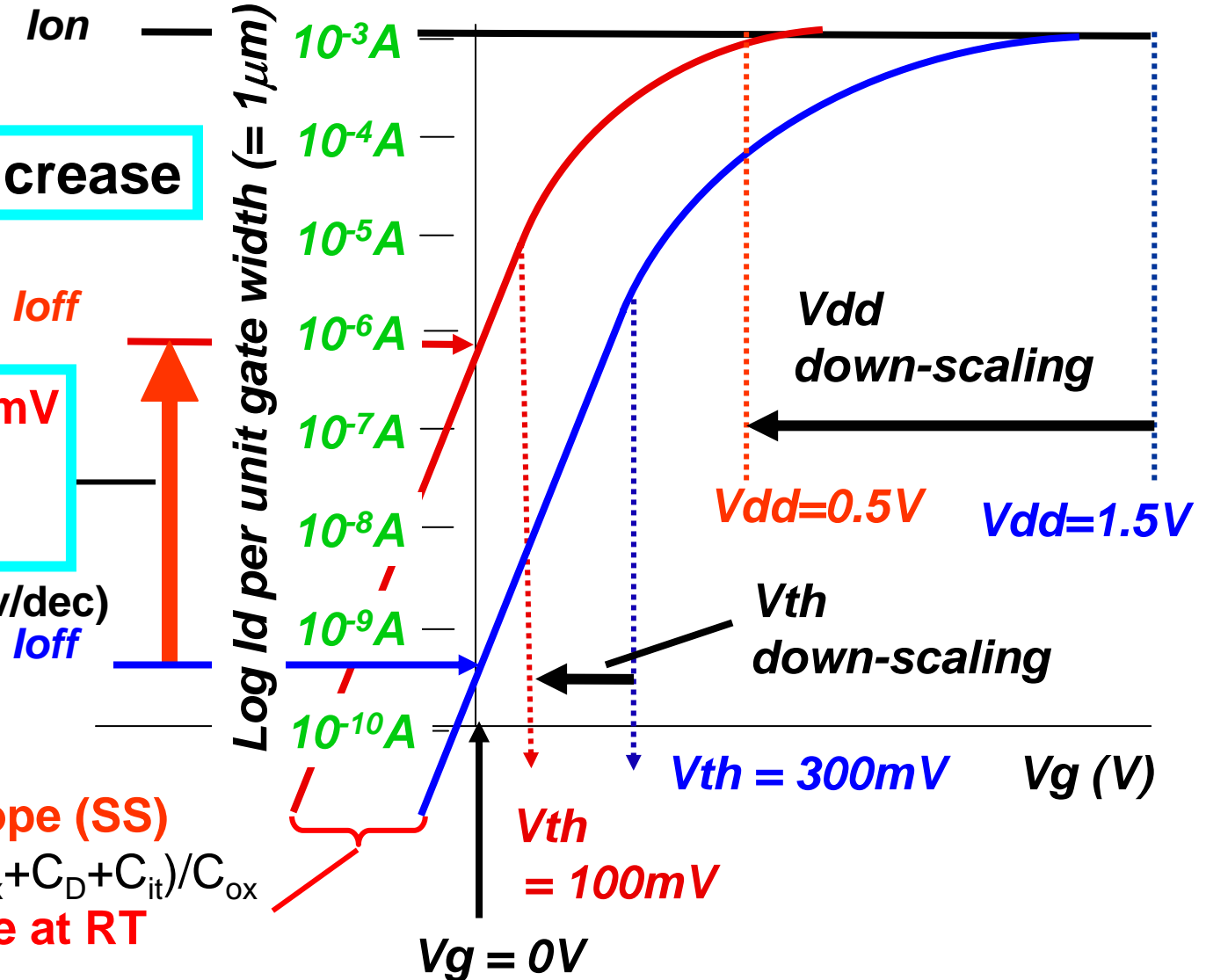
**Vth: 300mV → 100mV**  
**Ioff increases with 3.3 decades**

$$(300 - 100)\text{mV} / (60\text{mV/dec}) = 3.3 \text{ dec}$$

**Subthreshold slope (SS)**  
 $= (\ln 10)(kT/q)(C_{ox} + C_D + C_{it}) / C_{ox}$   
 $> \sim 60 \text{ mV/decade at RT}$

**SS value:**

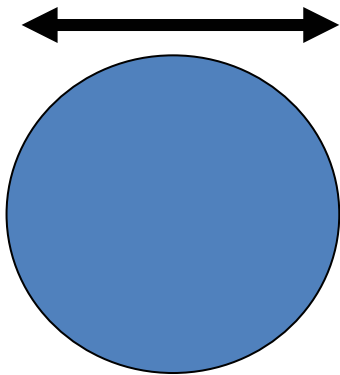
**Constant and does not become small with down-scaling**



**Prediction now!**

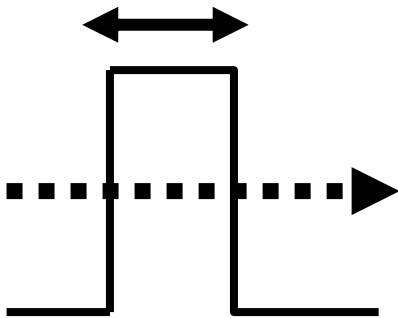
Electron wave length

**10 nm**



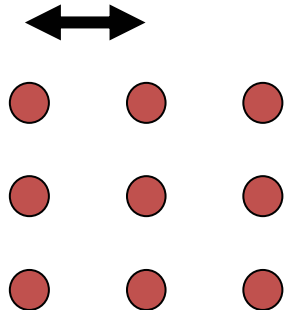
Tunneling distance

**3 nm**



Atom distance

**0.3 nm**



**Practical limit for integration**

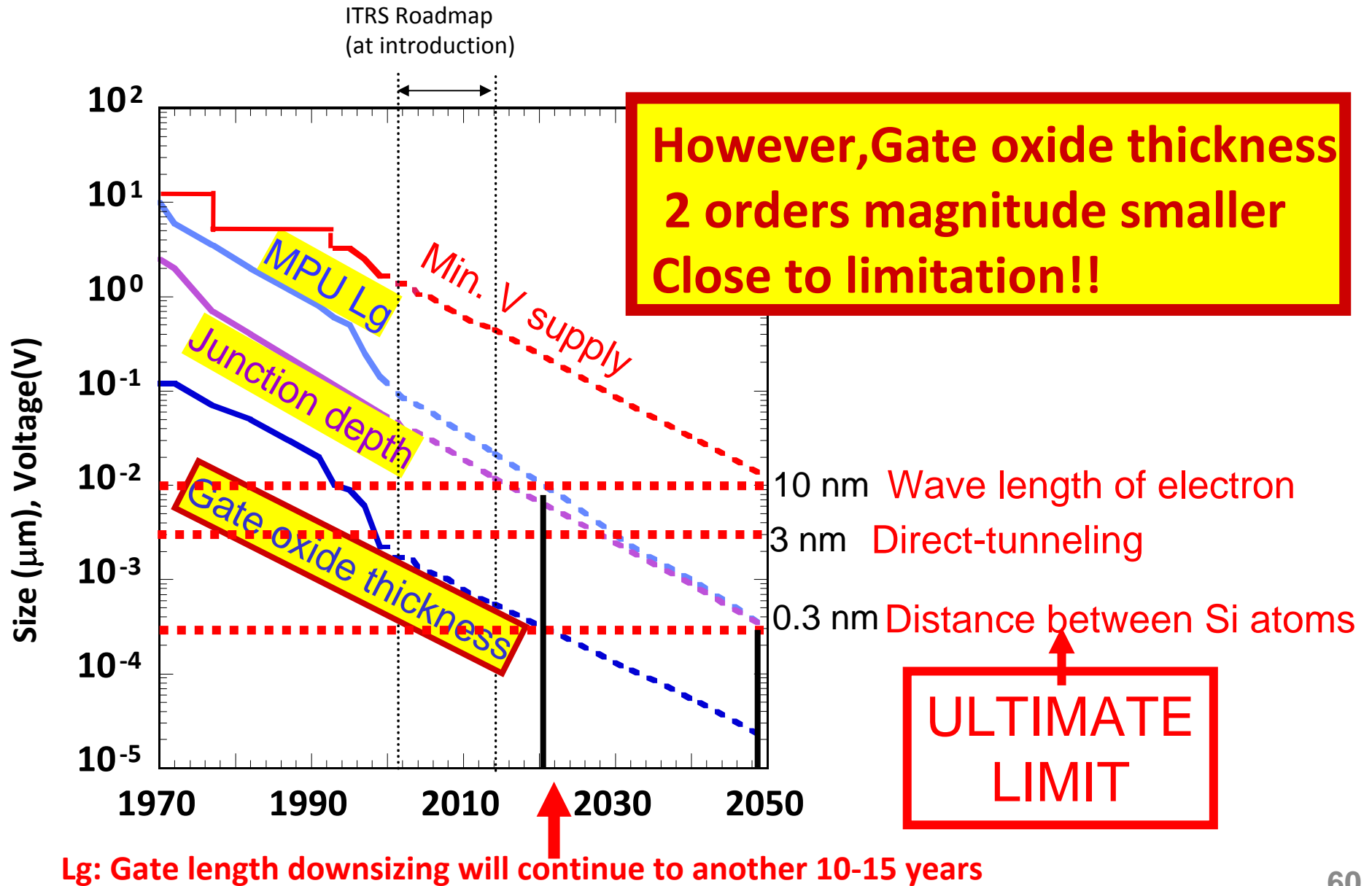
**$L_g = 5 \text{ nm?}$**

**MOSFET operation**

**$L_g = 2 \sim 1.5 \text{ nm?}$**

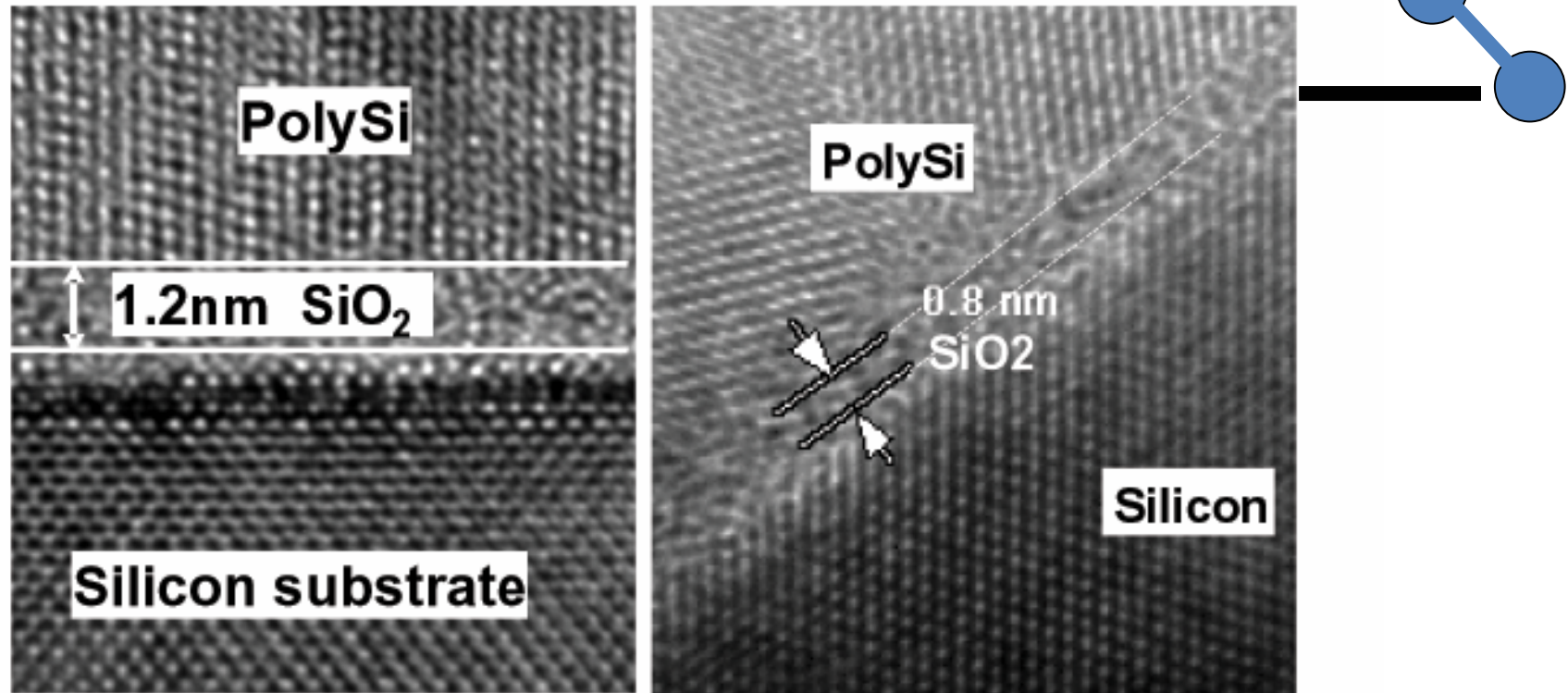
**Below this, no one knows future!**

# Ultimate limitation



# 0.8 nm Gate Oxide Thickness MOSFETs operates!!

*0.8 nm: Distance of 3 Si atoms!!*



- 1.2nm physical SiO<sub>2</sub> in production (90nm logic node)
- 0.8nm physical SiO<sub>2</sub> in research transistors

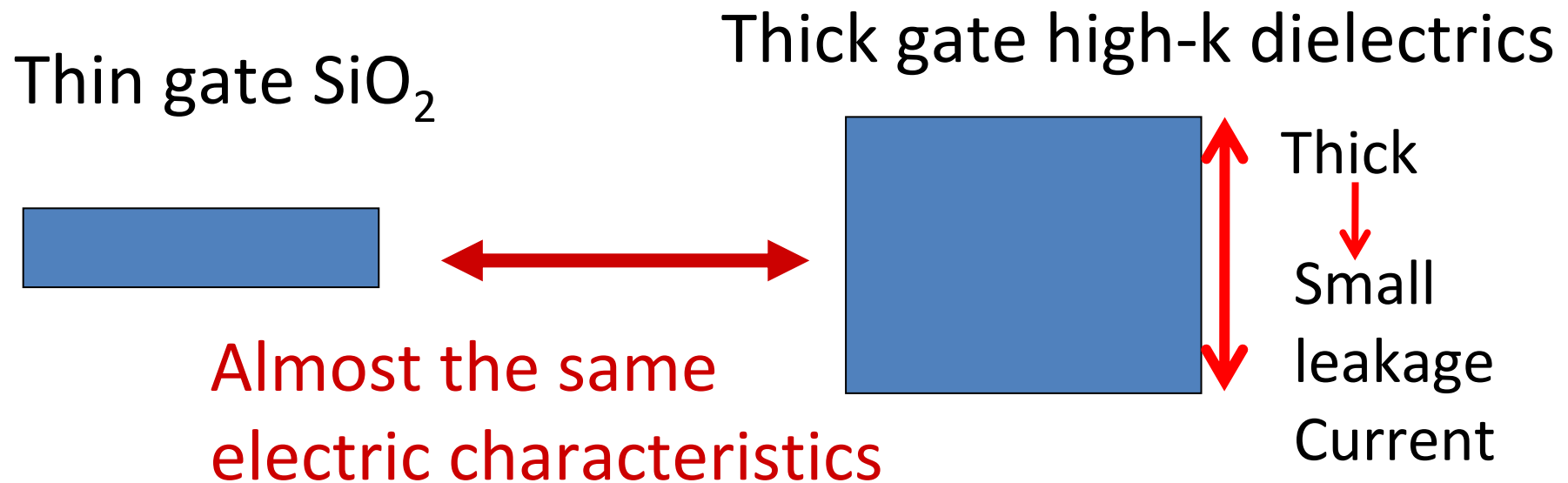
By Robert Chau, IWGI 2003

So, we are now in the limitation  
of downsizing?

Do you believe this or do not?

There is a solution! **K: Dielectric Constant**  
To use high-k dielectrics

---



However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO<sub>2</sub>!

## Choice of High-k elements for oxide

Candidates <span style="background-color: #e0ffff; padding: 2px;"> </span>														Gas or liquid at 1000 K											
Unstable at Si interface														Radio active											
H																				He					
Li	Be																			B	C	N	O	F	Ne
Na	Mg													Al	Si	P	S	Cl	Ar						
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr								
Rh	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rb	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe								
Cs	Ba		Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn								
Fr	Ra			Rf	Ha	Sg	Ns	Hs	Mt																
		La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu									
		Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr									

HfO<sub>2</sub> based dielectrics are selected as the first generation materials, because of their merit in

- 1) band-offset,
- 2) dielectric constant
- 3) thermal stability

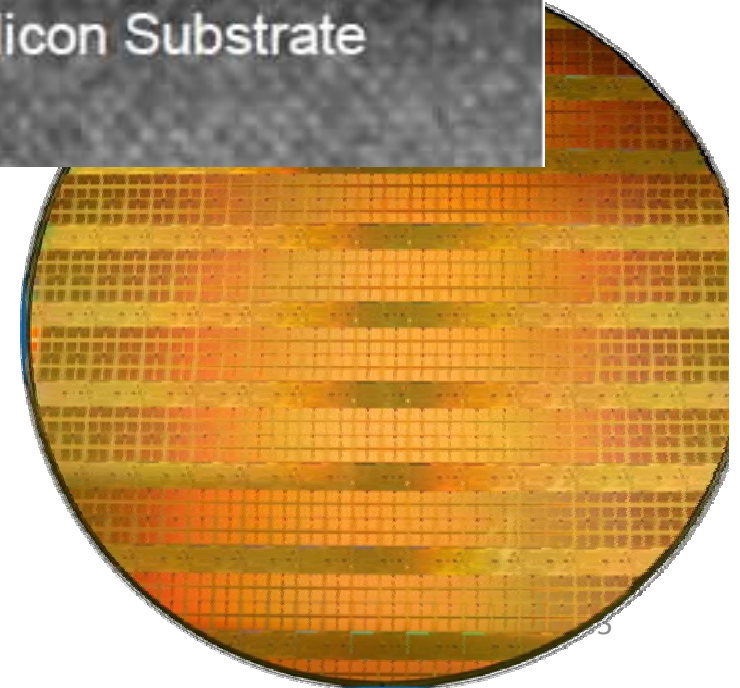
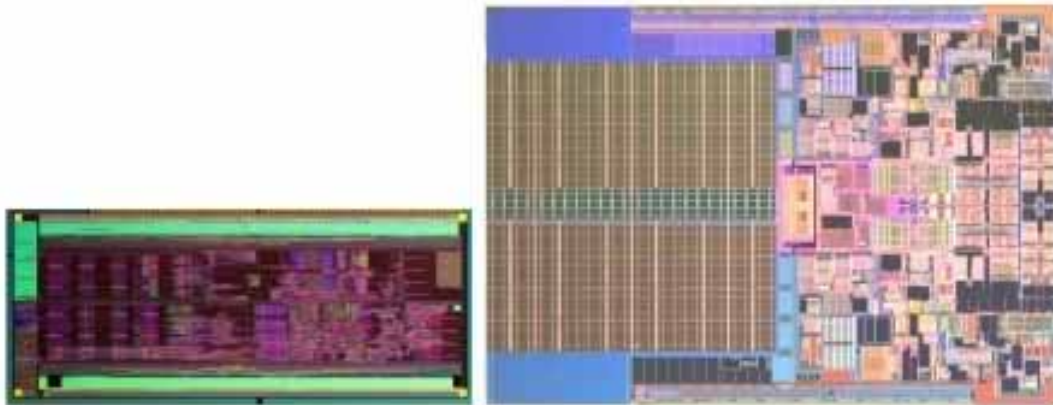
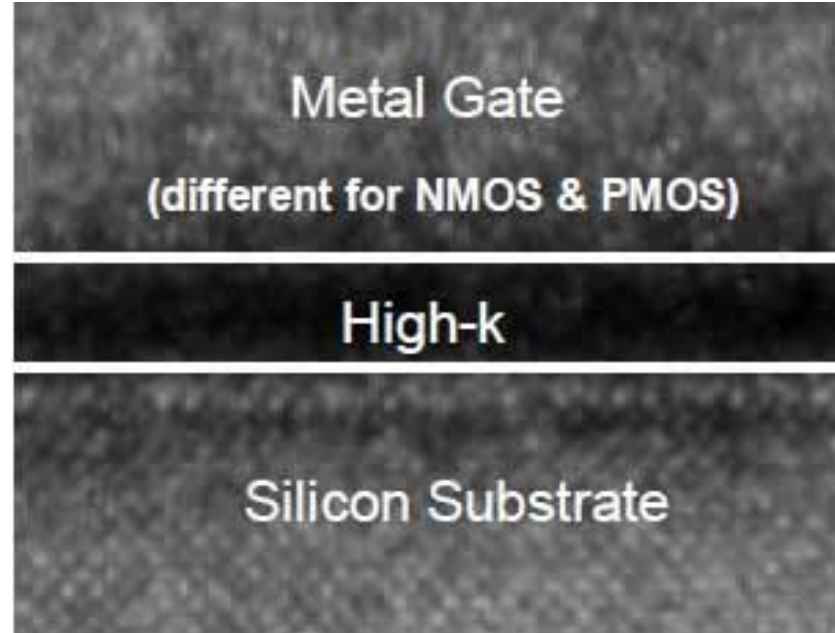
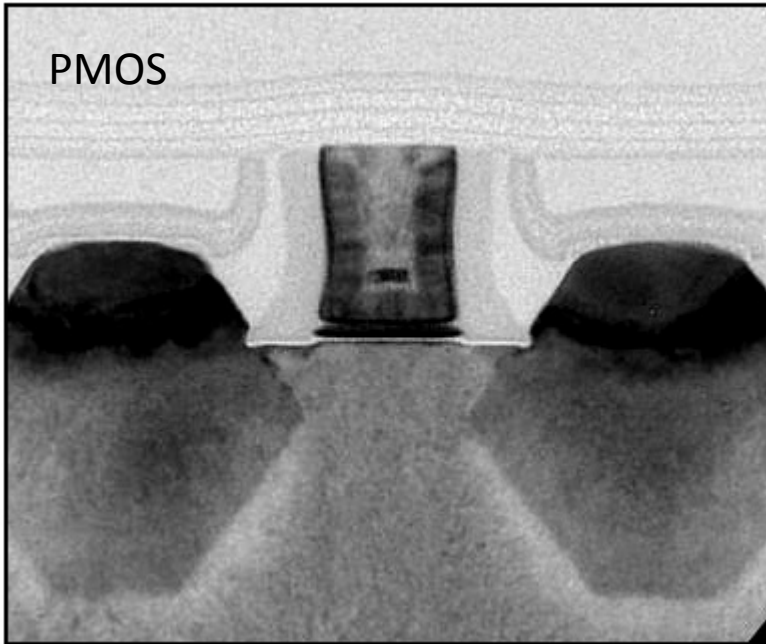
La<sub>2</sub>O<sub>3</sub> based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999  
Hubbard and Schlom, J Mater Res 11 2757 (1996)

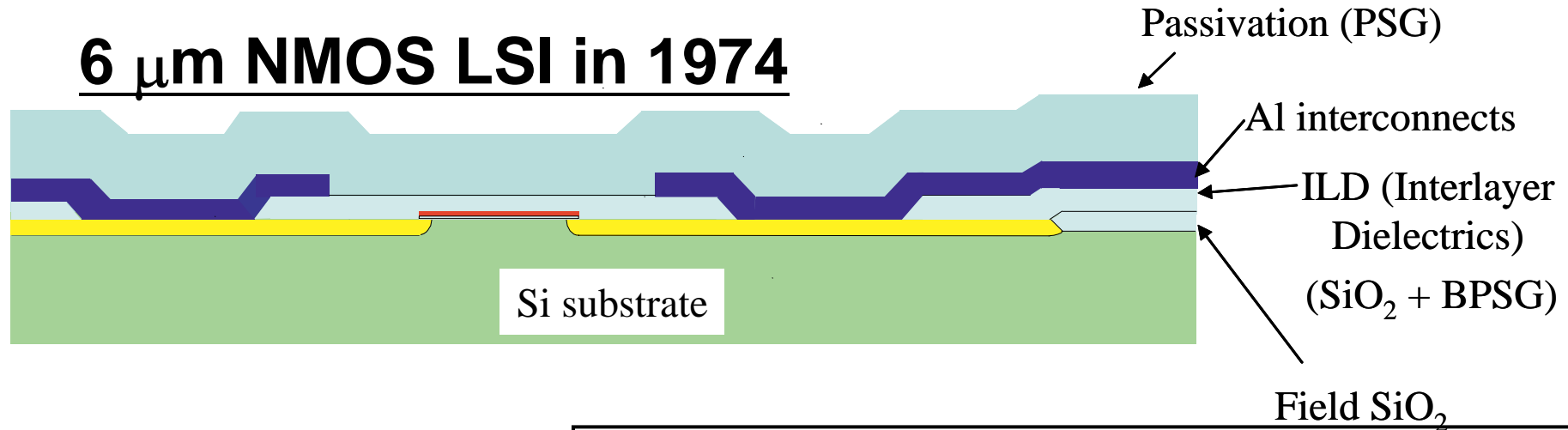


# High-k gate insulator MOSFETs for Intel: EOT=1nm

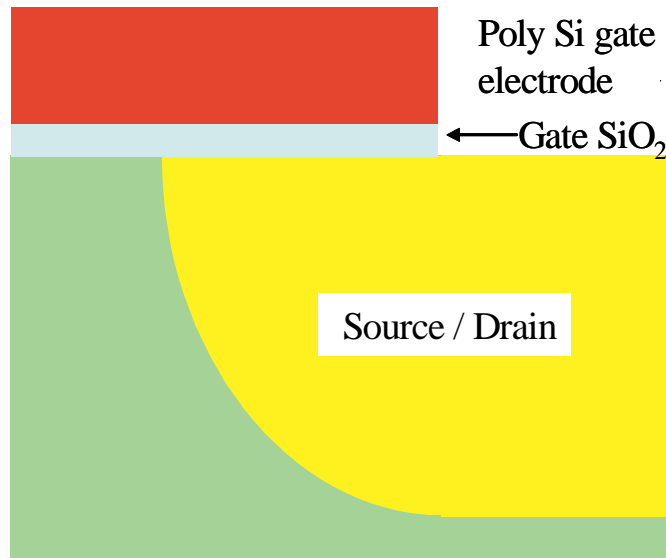
EOT: Equivalent Oxide Thickness



# 6 $\mu\text{m}$ NMOS LSI in 1974



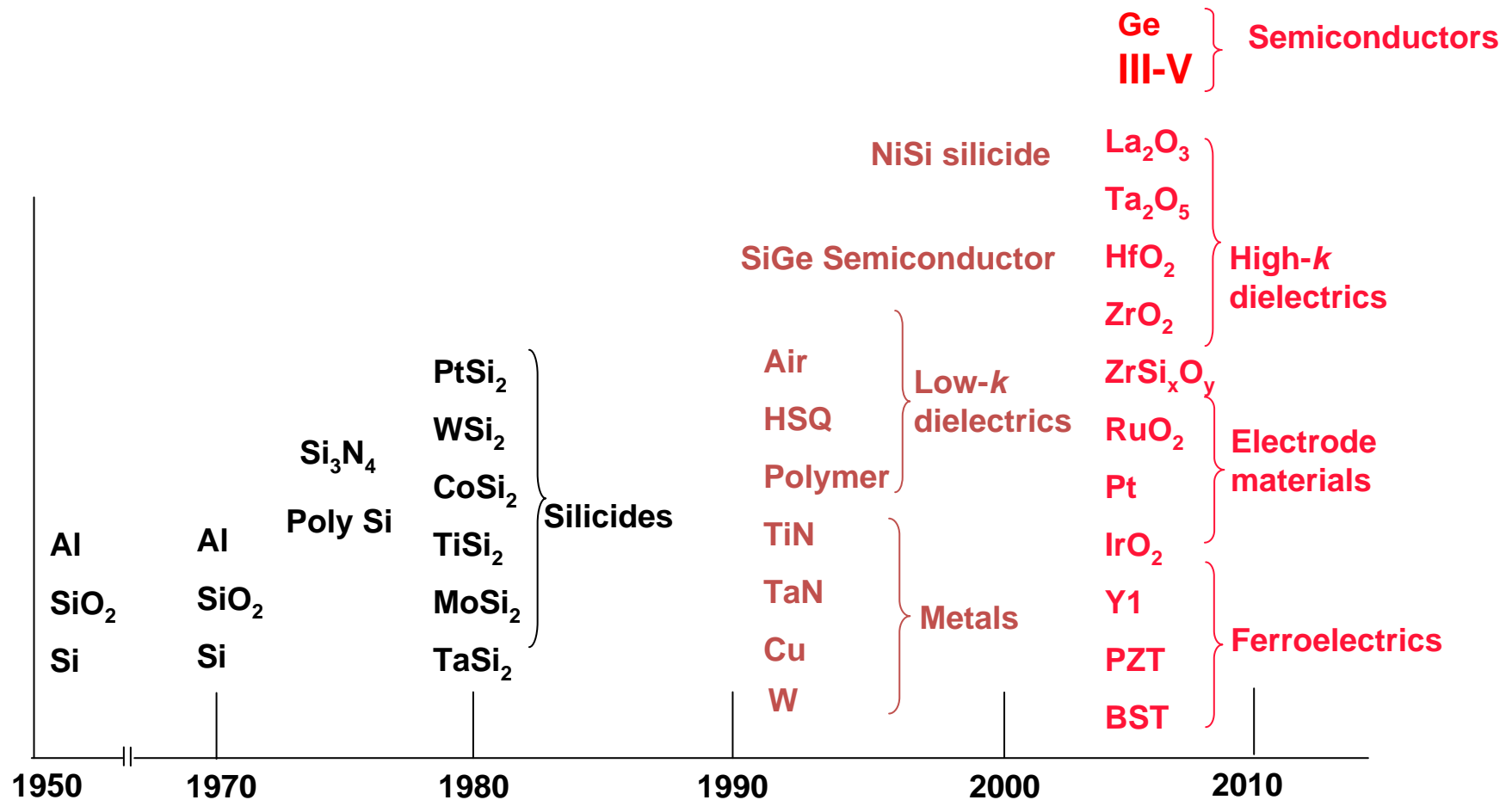
magnification  
↓



<u>Layers</u>	<u>Materials</u>	<u>Atoms</u>
1. Si substrate	1. Si	1. Si
2. Field oxide	2. SiO <sub>2</sub>	2. O
3. Gate oxide	3. BPSG	3. P
4. Poly Si	4. Al	4. B
5. S/D	5. PSG	5. Al
6. Interlayer		(H, N, Cl)
7. Aluminum		
8. Passivation		

# New materials

Just examples!  
Many other candidates



Y. Nishi, Si Nano Workshop, 2006,

(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)



**1970's**



**Toshiba Corporation**

300 mm Fab TSMC

**Now**



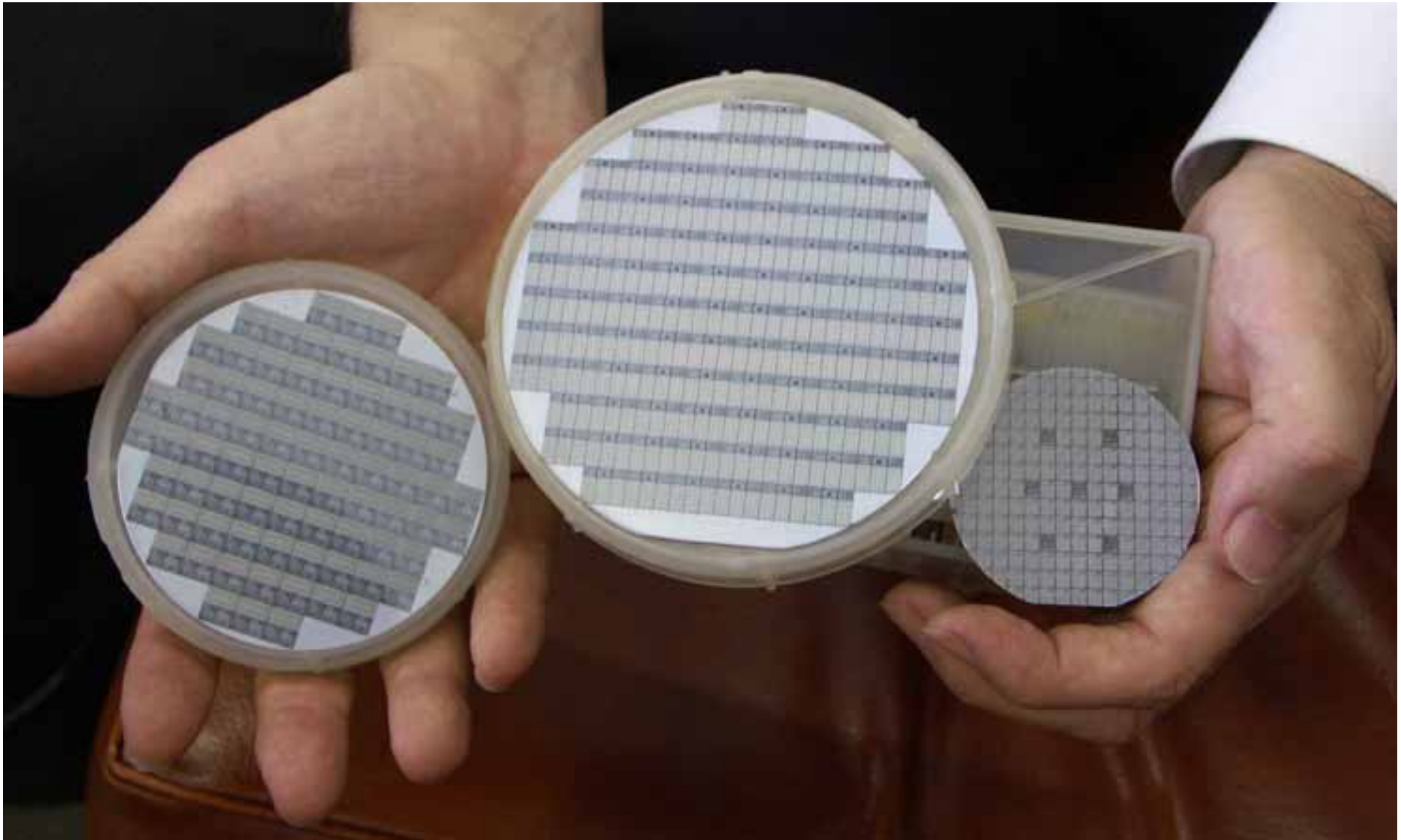
Toshiba Oita  
Works



300 mm Super clean  
room in  
Tsukuba, Selete

**In a future  
No person is necessary!**



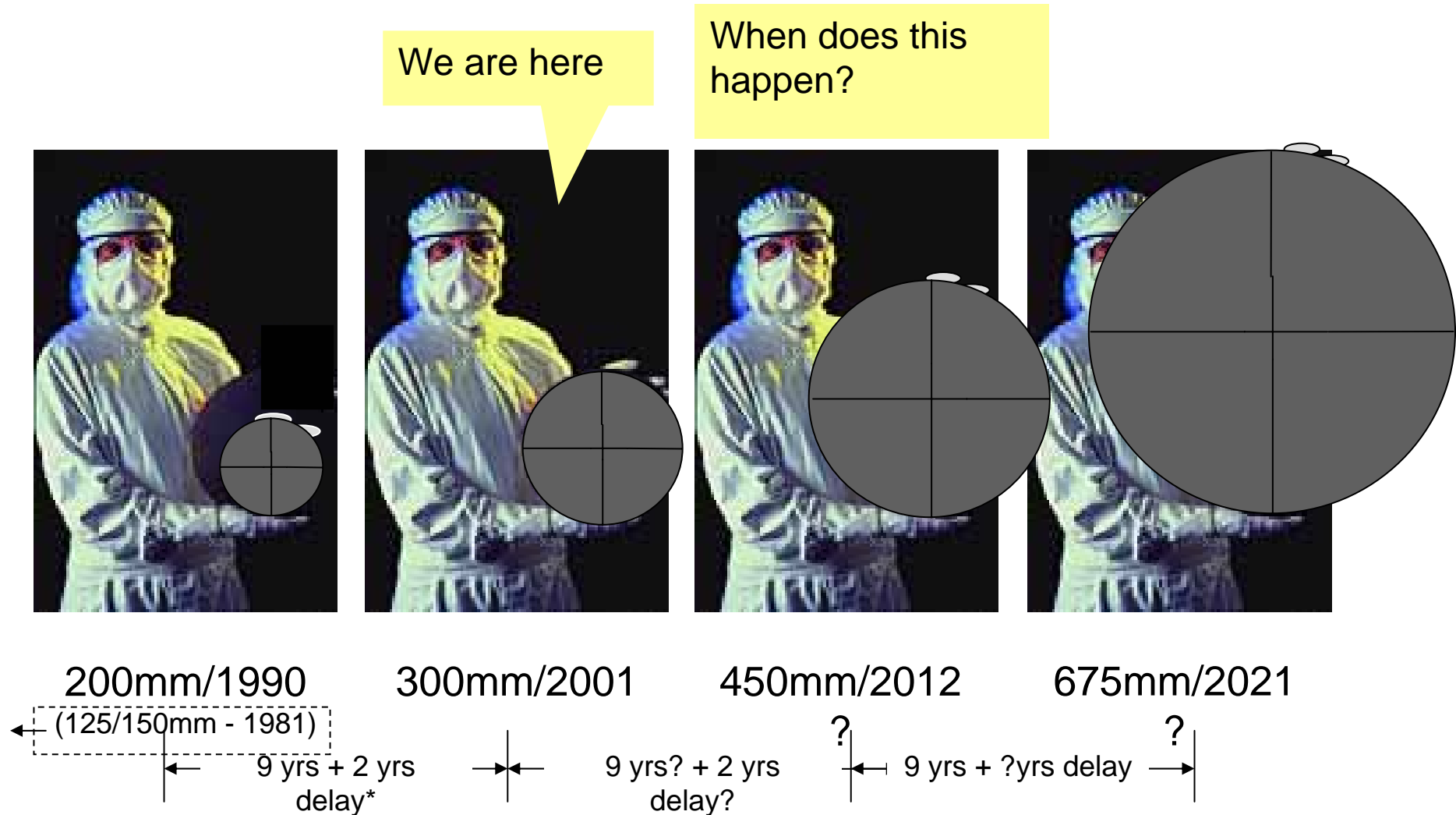


64k DRAM  
3 inch  
wafer

64k DRAM  
4 inch wafer  
**1980**

1k SRAM  
2 inch wafer  
**1974**

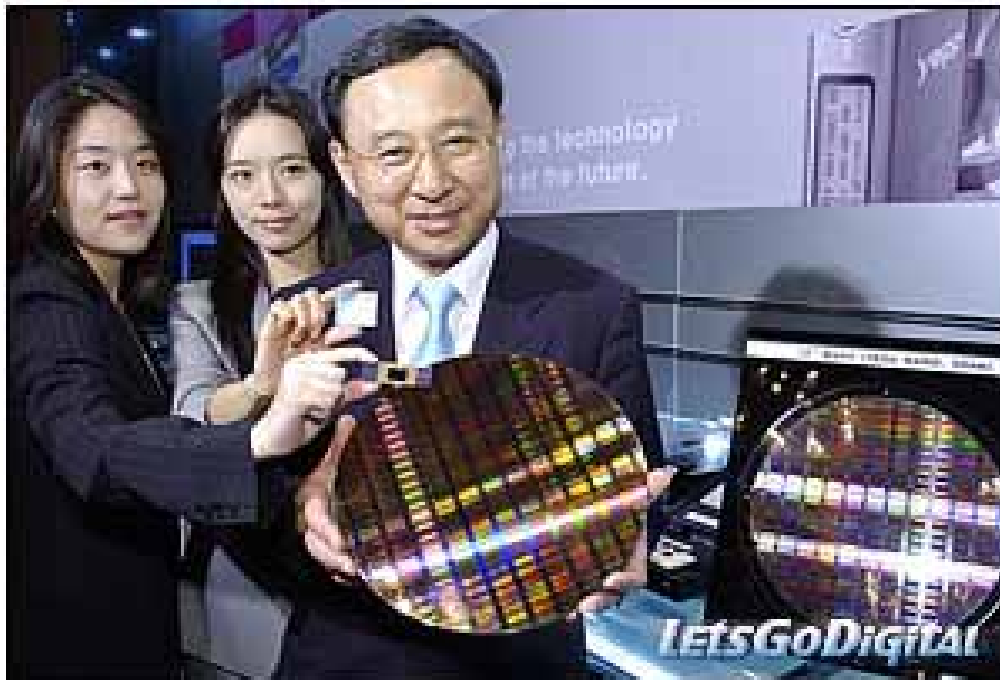
# When do we start planning for next wafer size transition?





# Now: After 50 Years from the 1st single MOSFETs

64Gbit, 32 Gb and 16Gb NAND,  
SAMSUNG



Already 64 Gbit:

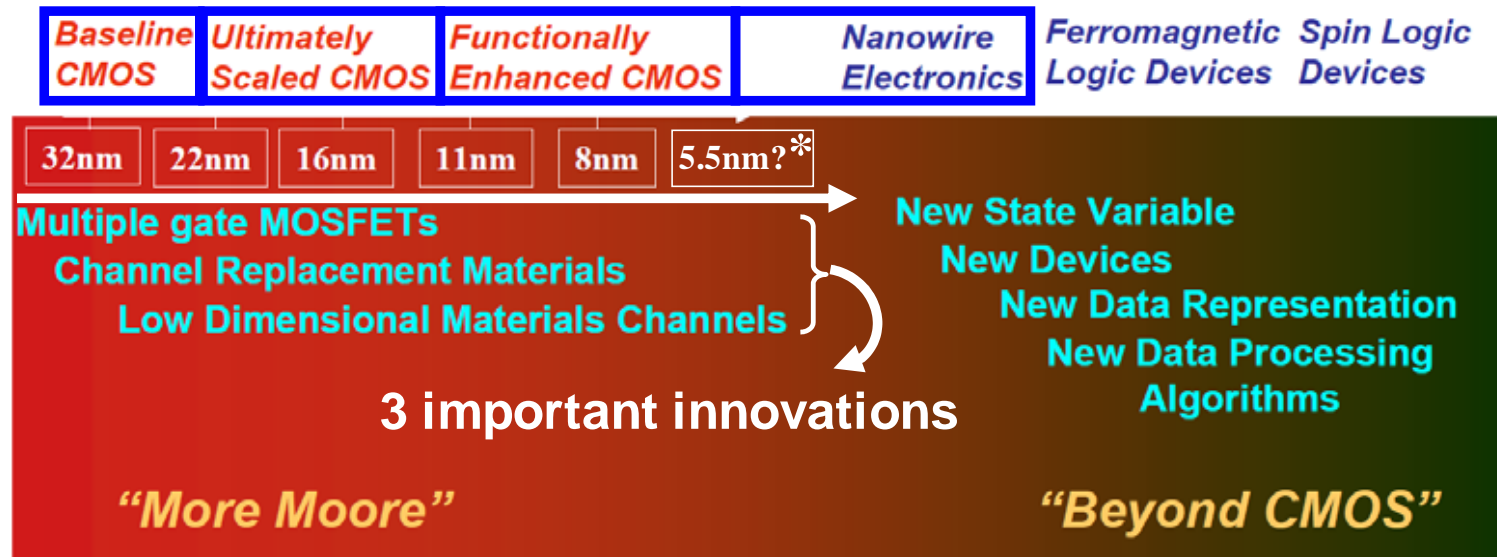
larger than that of world population  
comparable for the numbers of neurons  
in human brain

Samsung announced 256 Gbit will be produced

256Gbit: larger than those of # of stars in galaxies



- There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).
- Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher  $I_{d-sat}$  under low  $V_{dd}$ .
- Two candidates have emerged for R & D
  1. Nanowire/tube MOSFETs
  2. Alternative channel MOSFETs (III-V, Ge)
- Other Beyond CMOS devices are still in the cloud.

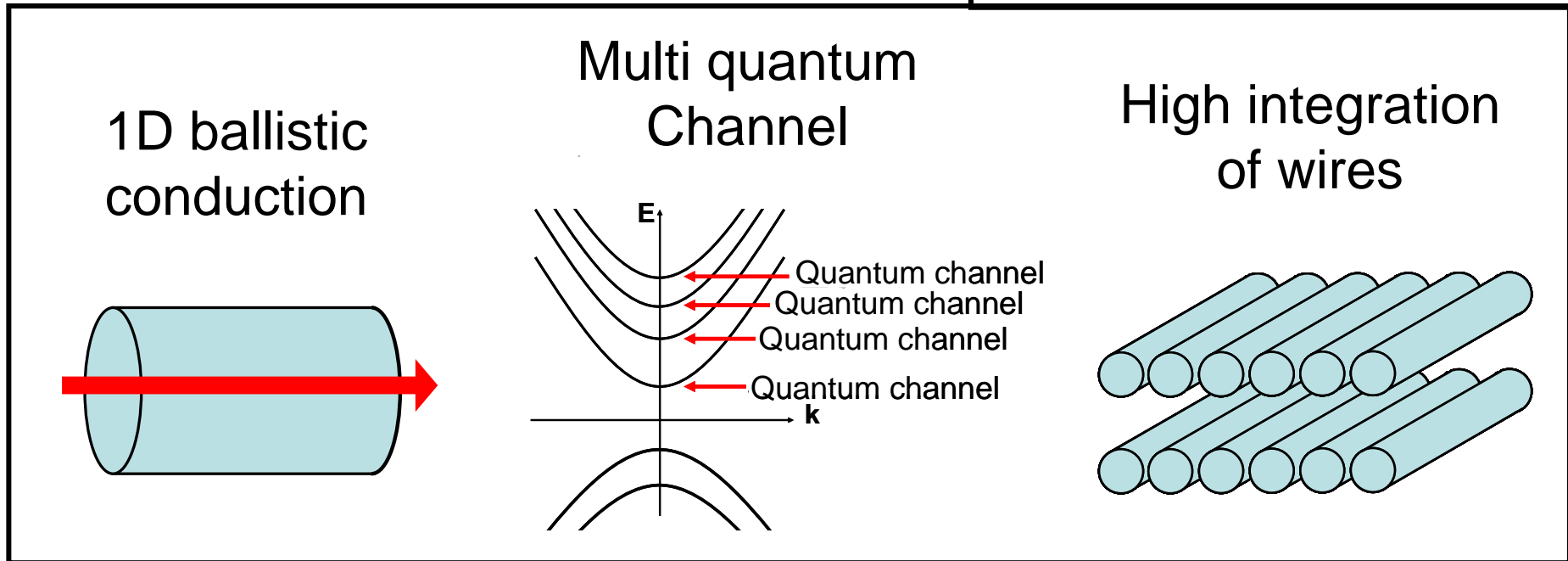
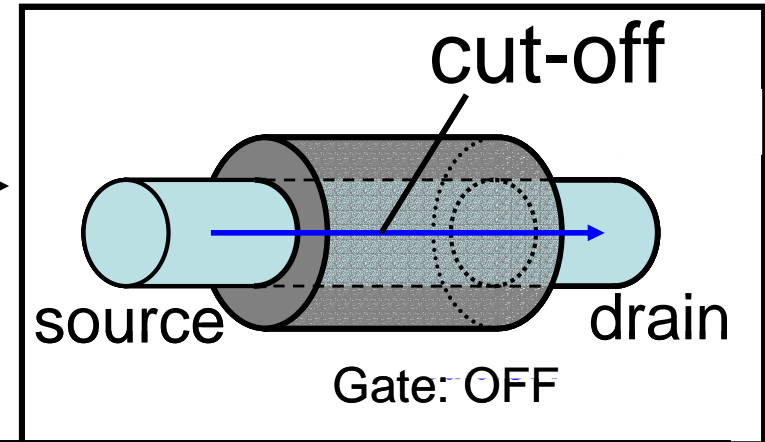


ITRS figure edited by Iwai

# Si nanowire FET as a strong candidate

after CMOS limitation

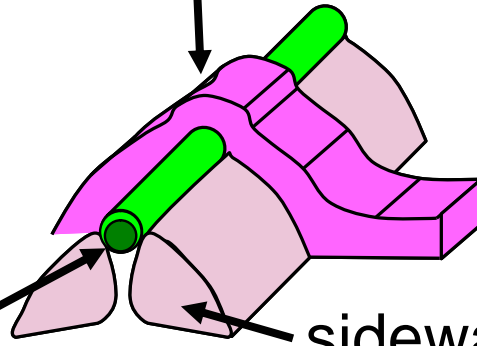
- 1. Compatibility with current CMOS process
- 2. Good controllability of  $I_{OFF}$
- 3. High drive current



TEM image  
10nm



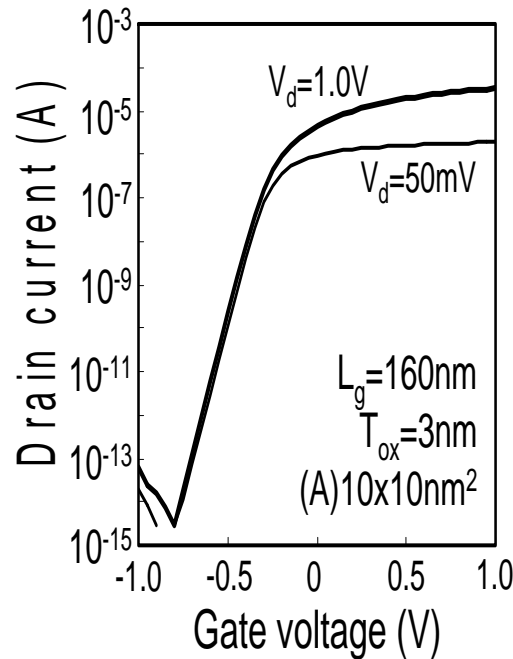
gate electrode



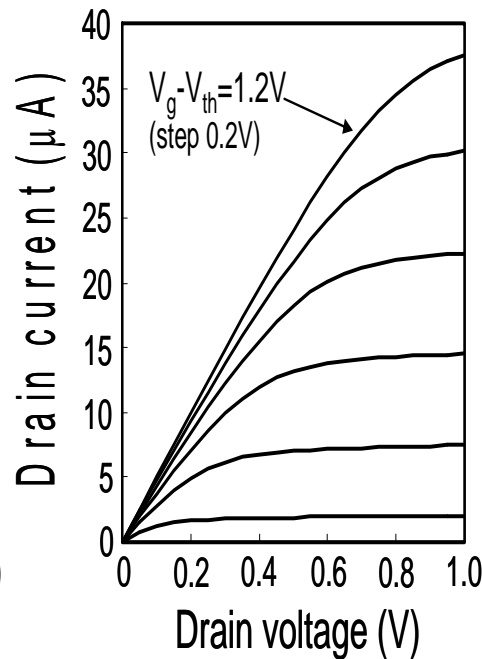
wire

sidewall

$L_g=160\text{nm}$ ,  $T_{ox}=3\text{nm}$



Nice cut-off



High drive

Advantage of Si nanowire

Large drive current

Spec. in 2019 by ITRS

$I_{ON}=2.3\text{mA}/\mu\text{m}$

$L_g=11\text{nm}$ ,  $T_{ox}=0.6\text{nm}$

Our nanowire FET

$I_{ON}=0.25\text{mA}/\mu\text{m}$  (with 2010  
Litho. tech.)

$L_g=160\text{nm}$

$T_{ox}=3.0\text{nm}$



With 2019 litho. tech.

$I_{ON}=2.3\text{mA}/\mu\text{m}$  will be  
obtained even with

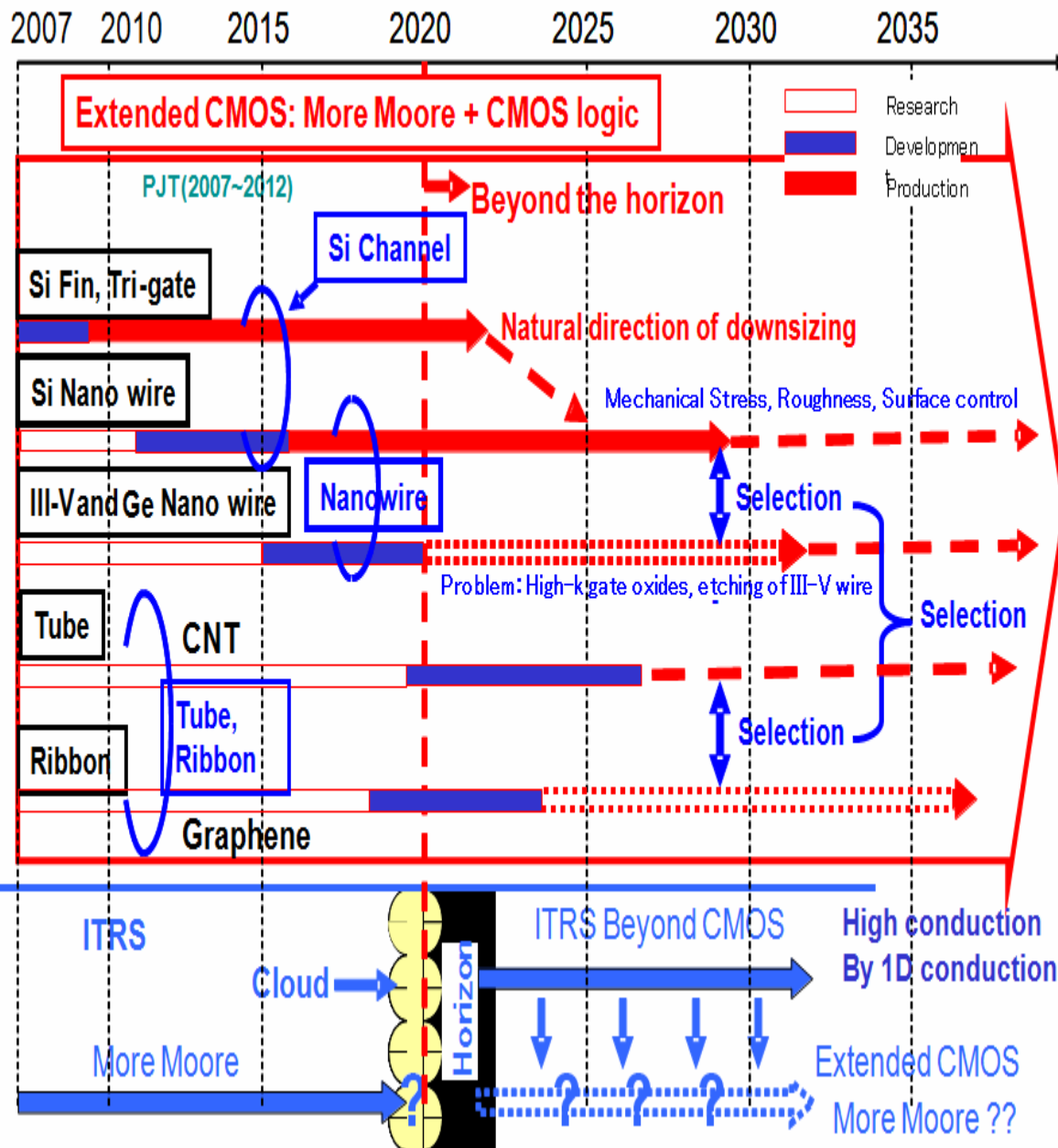
$L_g=80\text{nm}$  and  $T_{ox}=1.5\text{nm}$

by the courtesy of Professor H.Iwai

# Our roadmap for R & D

Source: H. Iwai, IWJT 2008

## Current Issues



### Si Nanowire

- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

### III-V & Ge Nanowire

- High-k gate insulator
- Wire formation technique

### CNT:

- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

### Graphene:

- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap

**System  
and  
Algorithm  
becomes  
more  
important  
!**

**Ultra small volume  
Small number of neuron cells  
Extremely low power**

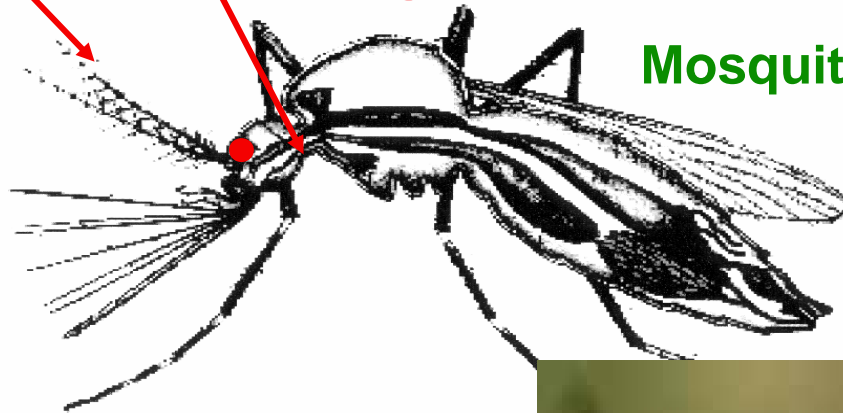
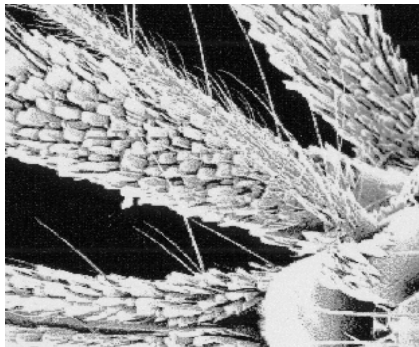
**Real time image processing  
(Artificial) Intelligence  
3D flight control**

**Mosquito**

**Brain**

**Sensor**

**Infrared  
Humidity  
CO<sub>2</sub>**



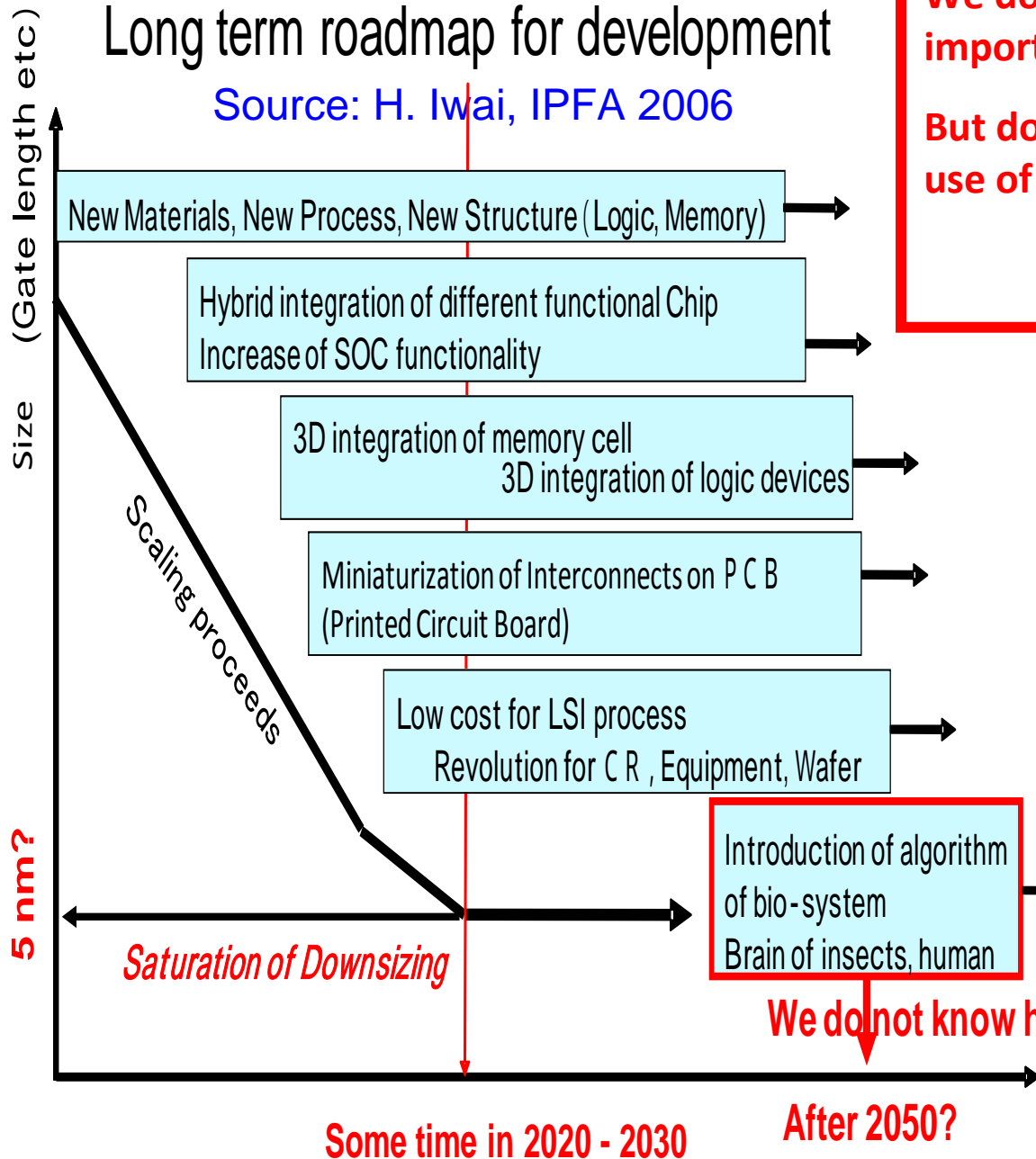
Dragonfly is further high performance



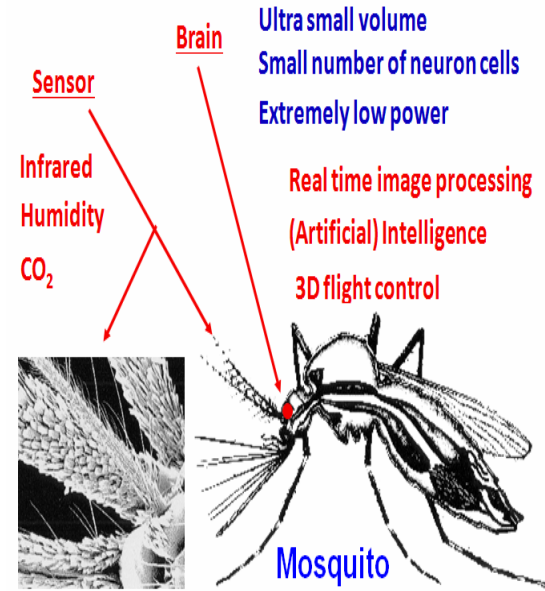
**But do  
not know  
how?**

# Long term roadmap for development

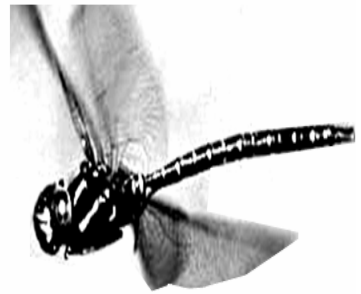
Source: H. Iwai, IPFA 2006



**We do know system and algorithms are important!**  
**But do not know how it can be by us for use of bio?**



**We do not know how?** Dragonfly brain has even further higher performance





Wanted: **CUSTOMERS**, who breathe, eat, and live in.....



**Global & Regional Political & Macro-Economic Environments**



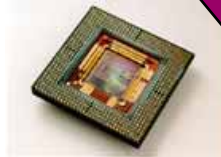
**Customer Demand**

**\$ 30,000B**

**Electronic End Equipment**

**\$ 850B**

**Semiconductors**



**\$ 300B**

**Semiconductor  
Equipment  
&  
Materials**

**\$ 50B**

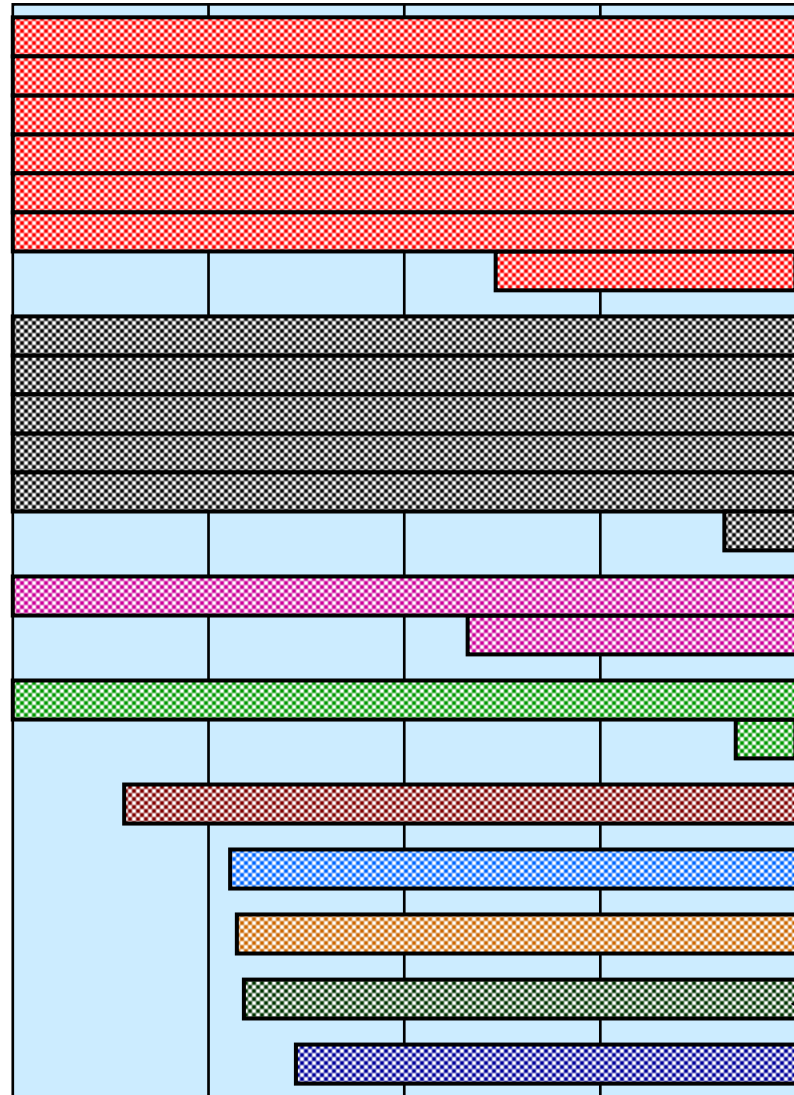


Sources: NASA.gov ; SEMI

*Data Source: UN*

population in million people

200 150 100 50 0



China

India

USA

Indonesia

Brazil

Russia

Pakistan

Bangladesh

Japan